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PHASE II TECHNICAL REPORT:

SOLID-STATE IMAGE SENSOR RESEARCH

By W.E. Davern, D.P. Dwyer, G.C. Gerhard,
R.E. Glusick, L.S. Jobin, C.W. Kim, A. Simone,
M.E. Seymour, R.D. Stewart and H.F. Windsor

March 1968

Prepared under Contract No. NAS 12-131 by
GENERAL ELECTRIC COMPANY
Electronics Laboratory, Syracuse, New York
and
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ELECTRONICS RESEARCH CENTER
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General Electric Company
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ABSTRACT

The development of a Solid State Image Sensor Array is described. The array consists of 50 InAs photodiodes fabricated in a monolithic structure. Each diode is connected, by thin-film leads, to external preamplifiers. The thin-film lead structure is part of a molded plastic substrate that permits the use of batch-fabricated leads, and provides the vacuum enclosure for frost-free operation at -80^{o}C.

Preamplifier circuits match the photovoltaic signal of the photodiodes to charge-storage capacitors, in order to provide frame time integration of the optical signal. The entire structure has been packaged for test and demonstration.

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I. INTRODUCTION AND SUMMARY

The continuing development of meteorological satellite systems has placed heavy demands upon infrared sensor technology in terms of higher sensitivity, greater uniformity, higher operating temperature, and lower cost. These goals, coupled with the further requirement for array operation of the IR sensors, has been the concern of the program "Solid State Image Sensor Research." This program, sponsored by NASA Electronics Research Center under contract NAS12-131, has been carried out by the Electronics Laboratory of the General Electric Company, Syracuse, New York, and the Missile and Space Division of the General Electric Company, Philadelphia, Pennsylvania.

The program has consisted of two phases: a study program extending from 15 June 1966 through 14 December 1966, and a device and system development program extending from 15 December 1966 through 31 October 1967.

During the study program, detectors and read-out systems were considered for use over the spectrum 0.4 micron through 15 microns. The study indicated that there were three specific spectral bands of interest and application to meteorological satellites, 0.4-0.7 micron, 2-5 microns, and 10-12 microns. Detectors and corresponding electronic read-out systems were evaluated for each of these bands. The combinations recommended for further development were:

0.4 - 0.7 μ: CdS and Si
2 - 5 μ: InAs and InSb
10 - 12 μ: PbSnTe

In each case, charge-storage mode of detector read-out was to be utilized, either directly or through an intermediate preamplifier.

At the conclusion of the study phase, it was ncessary to select one approach for the device development and fabrication phase of the program. That choice was InAs operating in the near-IR band. The primary reasons for this selection were:

1) High sensitivity: ($D^*_{\lambda_m} > 10^{11}$)
2) High operating temperature: ($200^{\circ}K$)
3) Availability of material.
4) Wavelength band with few sensor systems available at present time.

Details of the materials evaluated and the basis for the selection are given in the final report for this phase of the contract "Phase One Report, Solid State Image Sensor Research, NAS12-131."

Results of the fabrication and operation of the InAs array are contained in the present report. The task selected was the assembly and operation of an electronically scanned array of 50 detector diodes on a single array. The density of this array is 200 elements per inch.

The development of the detector array required that the methods of diffusion, surface passivation, and lead attachment be established. Device fabrication was initially developed for individual mesa structures and later for mesa diode arrays. These arrays were not compatible with a batch-fabricated lead approach; for this reason, planar arrays were developed. The processing procedures necessary to obtain both the mesa and planar arrays are described in Section II.C. of this report, while the array measurements are given in Section II.D.

In order to more effectively handle the 50 detectors on the single InAs chip, an interconnection technique was developed that provides all, or part, of the following functions: wafer support, thin-film interconnections replacing all flying leads, fan-out from device density to standard connector density, vacuum enclosure around array, vacuum feed-throughs for all 50 signal leads, and heat sink for cooling of detector elements. This structure, which is molded from an epoxy urethane mixture, is described in Section III.

Read-out of the individual photovoltaic detectors is accomplished with a preamplifier and a charge storage capacitor. Each preamp provides the necessary impedance matching between the detector and its associated capacitor. The integrated signal on the capacitor is then sampled by the commutator circuitry and made available for processing. Details of the scan system and the read-out circuitry are given in Section IV of this report. Packaging of the circuitry and the detector block is described in Section V.

Further application studies were performed during the second phase of the program, in order to ascertain the trade-off involved in using the 2-5 μ band in comparison with the 10-12 μ band, and also in comparing the performance of InAs, InSb, and a hypothetical InAsSb mixed-crystal detector. The results of this study indicate that, although the ultimate superiority of 8-12 micron detectors over 3-4 micron detectors for 300^{o}K targets is at least a factor of four, cryogenic requirements and detector production technology strongly favor the 3-4 micron band. Within the 3-4 micron band, similar comparisons exist between InAs and InSb. Sensitivity ratios favor the InSb by a factor of 2 to 3, while cooling temperatures favor the InAs. Details of these comparisons are given in Section VI.

The result of this program has been a demonstration of a complete solid-state line-scan camera system. The several key technical problem areas have been identified for further development. These include device uniformity, lead attachment, cooling effects on device, leads, and packaging, and preamplifier uniformity. It has been recommended to NASA-ERC that these problems receive further development, in order to advance the image sensor technology.

II. InAs DETECTORS AND ARRAYS

A. InAs PHOTODETECTOR

Detectors that operate in the infrared portion of the optical spectrum have not advanced as much as those in the visible. This is largely true because of the inavailability of small-bandgap semiconductor materials, although impurity absorption types of photoconductive detectors are available at relatively low temperatures. Most of the development in the intermediate infrared region has been devoted to InSb p-n junction photodetectors, and considerable progress in the device technology has been made. However, InAs photodetectors have received relatively less attention, and the basic technology has not yet been fully exploited.

P-n junction photodetectors can be formed by producing a thin p-type layer on an n-type single-crystal semiconductor. For InAs detectors, Cd is diffused into a Sn-doped n-type substrate. Contact can be made to the surface (part of the p-layer) and the base regions.

Consider the energy level diagram of a p-n junction detector, shown in Figure 1. Absorbed photons in the p-layer whose energy is greater than the

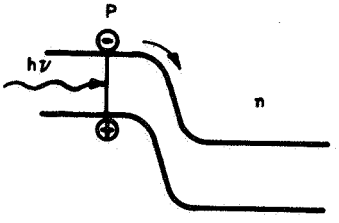


Figure 1. Energy Level Diagram of a p-n Junction

bandgap of the semiconductor produce electron-hole pairs. The minority carriers produced within a diffusion length will be diffused by a gradient to the junction. Thus, the electrons will be collected at the junction and be separated by the built-in electric field, leading to current flow in the external circuit if the contact leads are short-circuited.

The diffusion length is related to the mobility and lifetime. Since the electron mobility is higher than that of holes, the thin p-region was chosen as the optical absorption and carrier generation region, so that the minority carrier electrons would be diffused to the junction with longer diffusion length. The longer diffusion length means less recombination of the generated carriers and thus leads to higher optical signal sensitivity. The electron mobility for InAs is three orders of magnitude higher than that of holes.

In order to generate electron-hole pairs with appreciable efficiency, the incoming radiation must have an energy greater than the bandgap energy of the material. This results in a long-wavelength cutoff. For InAs, the E_g at room temperature is 0.35 electron volts, and the corresponding cutoff wavelength is 3.54 microns. InAs photodetectors generally require cooling to relatively low temperatures, and this, in turn, causes a shift to shorter cutoff wavelengths.

Sensitivity is also decreased as the wavelength decreases, because short wavelength radiation has a high absorption coefficient and thus is absorbed very near the surface. Carriers generated near the surface readily recombine, due to the surface and bulk recombinations,before they are collected at the junction.

P-n junction detectors can be operated either with or without reverse bias. The operation with bias is called photodiode mode; operation without bias is called photovoltaic mode.

In thermal equilibrium, a p-n junction has V-I characteristics given by

$$I_j = I_s (e^{qV/nkT} - 1) \qquad (1)$$

where I_j is the junction current, I_s is the saturation current, q is the charge, V is the potential drop across the junction, k is Boltzmann's constant, T is the temperature, and n is a factor that is unity for an ideal diode. The unilluminated V-I characteristics are shown in Figure 2, Curve 1.

When the detector is irradiated, the junction current is given by

$$I_j = I_s (e^{qV/nkT} - 1) - I_f \qquad (2)$$

where I_f is the current induced by the optical radiation. The V-I characteristics are shown in Figure 2 as Curve 2. The intersection with the current axis corresponds to the short-circuit current, whereas intersection with the voltage axis corresponds to the open-circuit voltage.

If the detector is operated in the photodiode mode, that is, biased in reverse direction, the current and voltage are shown as those at point x in Figure 2; V_b and I_s. Radiation of the proper wavelength falling on the detector causes an increase in leakage current over the top of the barrier, the reverse current changing to point y. This increase in current is detected by placing a small load resistor in series with the detector and measuring the increase in voltage appearing across it in the presence of optical radiation on the detector.

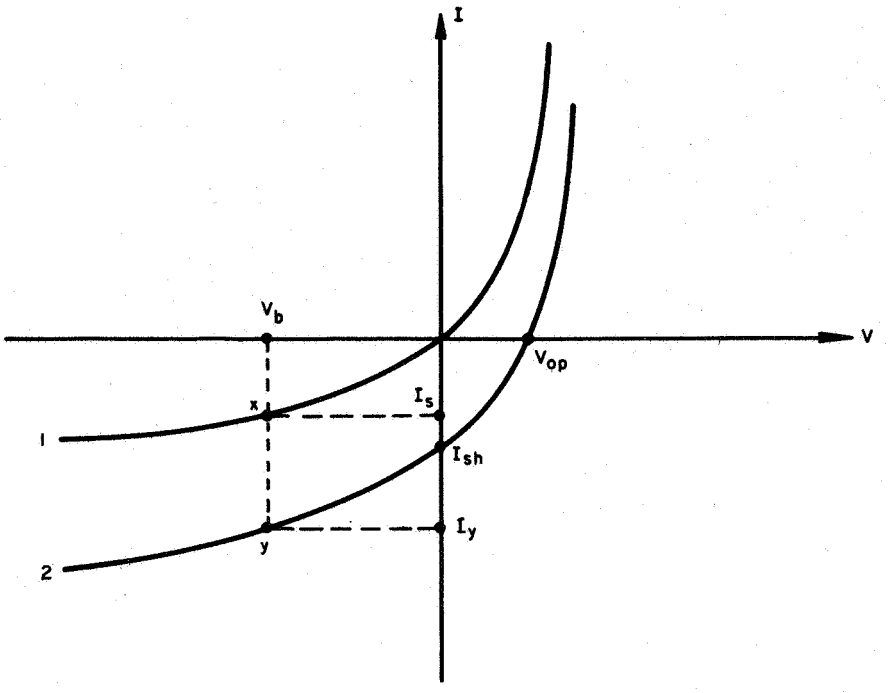


Figure 2. V-I Characteristics

The fundamental shot noise associated with an ideal photodiode can be expressed in terms of shot noise for each current:

$$i_n^2 = 2q\Delta f(I_s + I_f) \qquad (3)$$

where Δf is bandwidth. Note that the photodiode noise is a function of the saturation current and the signal current of the diode in the dark.

Since the saturation current of InAs junctions is generally high and the shot noise increases, it appears that the photovoltaic mode of operation leads to higher sensitivity. In the photovoltaic mode of operation, the detector has a low impedance, and special attention must be given to the associated preamplifier.

B. PHOTOVOLTAIC DIODE DESIGN

In the photovoltaic mode of operation, the impedance of the diode is small, and therefore, the detector is assumed to be a voltage source. Detection of the optical signal can be made by measuring the open-circuit voltage. An increase in voltage is related to the optical signal power.

Consider a model, shown in Figure 3, with N, the number of photons/cm^2sec, incident upon the surface x = 0. The relationship between N and the incident intensity, W(λ)(watts/cm^2), is given by

$$N(\lambda) = 5.04 \times 10^{18} \lambda\, W(\lambda) \tag{4}$$

for λ expressed in microns. If each photon absorbed is assumed to produce one free electron-hole pair, then the generation rate at any plane, a distance x below the surface, is given according to Lambert's law,

$$g(x, \lambda) = \alpha(\lambda)\, N(\lambda)\, e^{-\alpha(\lambda)x} \tag{5}$$

where $\alpha(\lambda)$ is the absorption coefficient of the material used.

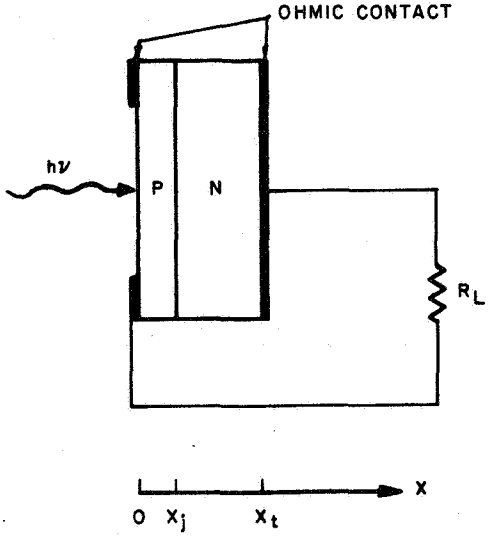


Figure 3. Model for a p-n Junction Photodetector

The continuity equation for electrons in the p-region, for the case of steady-state (if the carrier lifetime is much smaller than the response time) and monochromatic photon excitation is

$$\frac{n_o - n}{\tau_e} + \frac{1}{q}\frac{dJ_e}{dx} + g(x,\lambda) = 0 \quad , \tag{6}$$

and a similar expression applies for holes in the n-region, viz.

$$\frac{p_o - p}{\tau_h} - \frac{1}{q}\frac{dJ_h}{dx} = 0 \tag{7}$$

where p and n are the hole and electron densities, p_o and n_o are the equilibrium densities, and τ_h and τ_e are the minority carrier lifetimes for holes and electrons, respectively. Note that the p-region is sufficiently wide so that all the photons are absorbed in the p-region.

The operating principles of collecting the photo-generated charge carriers depend on the charge transport mechanisms. If the carriers are generated in a non-depletion region and are transported by diffusion to the junction, the minority carrier current densities, J_e and J_h, are given by

$$J_e = qD_e \frac{dn}{dx} \tag{8}$$

$$J_h = -qD_h \frac{dp}{dx} \tag{9}$$

where D_e and D_h are the diffusion constants of the minority carriers, respectively.

At $x = 0$, if the contact to the illuminated surface is a perfect ohmic contact, no minority carriers are injected into, or extracted from the region, and the only minority carriers lost are those that recombine at the surface of the p-region. That is,

$$qD_e \left.\frac{dn}{dx}\right|_{x=0} = qS\left[n(o) - n_o\right] \tag{10}$$

where S is the surface recombination velocity.

At the junction $x = x_j$, the boundary conditions depend on the manner in which the diode is used. If the diode is short-circuited so that a perfect sink for minority carriers exists,

$$n(x_j) = p(x_j) = 0 \quad . \tag{11}$$

If the diode is connected to a load or open-circuited, the carriers at the junction are described by Boltzmann statistics as follows:

$$n(x_j) = n_o e^{\beta V} \quad , \tag{12}$$

$$p(x_j) = p_o e^{\beta V} \tag{13}$$

where $\beta = q/kT$ and V is the reduction of the equilibrium barrier height of the p-n junction due to the generation of nonequilibrium carrier concentrations by the incident radiation.

At the back surface, $x = x_t$ (the sample thickness), the excess carrier density is equal to zero;

$$p = p_o \quad . \tag{14}$$

Equations (12) and (13) can be expanded in power series.

$$n - n_o = n_o\left\{\beta V + \frac{(\beta V)^2}{2!} + \frac{(\beta V)^3}{3!} + \cdots\right\} \quad , \tag{15}$$

$$p - p_o = p_o\left\{\beta V + \frac{(\beta V)^2}{2!} + \frac{(\beta V)^3}{3!} + \cdots\right\} \quad . \tag{16}$$

If the generated voltage is much smaller than kT/q, the above equations can be approximated to the first term, that is,

$$n - n_o \cong n_o \beta V \quad , \tag{17}$$

$$p - p_o \cong p_o \beta V \quad . \tag{18}$$

At $T = 77^{\circ}K$, $kT/q = 6.64$ mv, the voltage level of a practical InAs detector is usually much smaller than this voltage, and therefore the above approximation should be hold under low intensity radiation. It should be noted that under this condition the voltage is directly proportional to the excess carrier concentrations generated by the incident radiation.

Substitution of (5) and (8) into (6) yields

$$\frac{d^2 n}{dx^2} - \frac{(n - n_o)}{D_e T_e} = -\frac{\alpha N}{D_e} e^{-\alpha x} \quad . \tag{19}$$

The general solution of this inhomogeneous differential equation is

$$n - n_o = A \cosh \frac{x}{L_e} + B \sinh \frac{x}{L_e} - \frac{\alpha T_e N}{\alpha^2 L_e^2 - 1} e^{-\alpha x} \quad . \tag{20}$$

The constants A and B can be determined from the boundary conditions (10) and (17). The final solution for the excess minority carrier concentration in the p-region is then given by

$$n - n_o = \frac{\left\{n_o\beta D_e(\alpha^2 L_e^2 - 1)V + \alpha T_e D_e N e^{-\alpha x_j}\right\}\cosh\frac{x}{L_e} + \left\{n_o\beta S L_e(\alpha^2 L_e^2 - 1)V + \alpha T_e S L_e N e^{-\alpha x_j}\right\}\sinh\frac{x}{L_e} + \alpha T_e L_e(\alpha D_e + S)N \sinh\frac{(x_j - x)}{L_e}}{(\alpha^2 L_e^2 - 1)\left(S L_e \sinh\frac{x_j}{L_e} + D_e \cosh\frac{x_j}{L_e}\right)} - \frac{\alpha T_e N}{\alpha^2 L_e^2 - 1} e^{-\alpha x} \quad . \tag{21}$$

Likewise the excess holes in the n-region can be determined from (7) and (9) with the boundary conditions (14) and (18), and are given by

$$p - p_o = \frac{p_o\beta \sinh\frac{(x_t - x)}{L_h} V}{\sinh\frac{(x_t - x_j)}{L_h}} \quad . \tag{22}$$

The current density of electrons follows from equations (8) and (21):

$$J_e = qD_e\left.\frac{dn}{dx}\right|_{x=x_j} = \frac{qD_e\left\{\left[n_o\beta D_e(\alpha^2 L_e^2 - 1)V + \alpha T_e D_e N e^{-\alpha x_j}\right]\frac{\sinh\frac{x_j}{L_e}}{L_e} + \left[n_o\beta S L_e(\alpha^2 L_e^2 - 1)V + \alpha T_e S L_e N e^{-\alpha x_j}\right]\frac{\cosh\frac{x_j}{L}}{L_e} - \frac{\alpha T_e L_e(\alpha D_e + S)N}{L_e}\right\}}{(\alpha^2 L_e^2 - 1)\left(S L_e \sinh\frac{x_j}{L_e} + D_e \cosh\frac{x_j}{L_e}\right)} + \frac{qD_e(\alpha^2 T_e N) e^{-\alpha x_j}}{\alpha^2 L_e^2 - 1} \quad . \tag{23}$$

Similarly, the current density of holes in the n-region is evaluted at $x = x_j$

$$J_h = -qD_h\left.\frac{dp}{dx}\right|_{x=x_j} = \frac{qp_o\beta D_h V}{L_h \tanh\frac{(x_t - x_j)}{L_h}} \quad . \tag{24}$$

The total current density of the diode is the sum of the two current densities;

$$J = J_e + J_h \quad . \tag{25}$$

The open-circuit voltage of the photovoltaic diode can be determined by setting the total current J=0. This leads to a relationship between the optical intensity (power) and the measuring voltage.

$$V = \frac{\alpha T_e\left\{L_e(\alpha D_e+S)-\left[D_e\sinh x_o+SL_e\cosh x_o+\alpha L_e(SL_e\sinh x_o+D_e\cosh x_o)\right]e^{-\alpha x_j}\right\}}{\beta(\alpha^2L_e^2-1)\left\{n_o(SL_e\cosh x_o+D_e\sinh x_o)+\dfrac{p_oL_eD_h(SL_e\sinh x_o+D_e\cosh x_o)}{L_hD_e\tanh\dfrac{(x_t-x_j)}{L_h}}\right\}}N \qquad (26)$$

where $x_o = x_j/L_e$.

Note that the voltage of the diode generated by the absorption of photons is linearly proportional to the number of the incident photons. This linear relationship should be valid as long as the photo-generated voltage is much less than kT/q.

In order to maximize the voltage of the photovoltaic diode, it is necessary to minimize the denominator and to maximize the numerator of equation (26). To decrease the denominator is to decrease n_o and p_o, that is, to dope both p and n regions as heavily as possible. To increase the numerator, it is required to increase the electron lifetime T_e and diffusion length L_e. Therefore, for an optimum operation in the photovoltaic mode, it is necessary that the minority carrier concentrations should be as low as possible and that the electron mobility and lifetime should be as high as possible.

The dynamic resistance R of the diode, defined as the slope of current-voltage curve at near zero voltage, is given by

$$\frac{1}{R} = A\left.\frac{dJ}{dV}\right|_{V\simeq 0} \qquad (27)$$

where A is the diode area and thus R is

$$R = \frac{L_e\left(SL_e\sinh\dfrac{x_j}{L_e}+D_e\cosh\dfrac{x_j}{L_e}\right)}{q\beta A\left\{n_oD_e\left(D_e\sinh\dfrac{x_j}{L_e}+SL_e\cosh\dfrac{x_j}{L_e}\right)+\dfrac{p_oD_hL_e\left(SL_e\sinh\dfrac{x_j}{L_e}+D_e\cosh\dfrac{x_j}{L_e}\right)}{L_h\tanh\dfrac{(x_t-x_j)}{L_h}}\right\}}. \qquad (28)$$

The thermal noise voltage for unit bandwidth is

$$V_n = \sqrt{4kTR} \quad . \qquad (29)$$

From equation (4) N can be expressed in terms of the radiant power P_λ

$$N = 5.04 \times 10^{18} \lambda \frac{P_\lambda}{A} , \tag{30}$$

for P_λ expressed in watts, A in cm^2, and λ in microns.

Equating the open circuit voltage (26) with the thermal noise voltage (29) and using equation (30), the radiant power P_λ can be determined from the equality. D^*_λ is defined by

$$D^*_\lambda = \frac{\sqrt{A}}{P_\lambda} . \tag{31}$$

Therefore, D^*_λ is given by

$$D^*_\lambda = \frac{5.04\times 10^{18}\lambda\alpha T_e\left\{L_e(\alpha D_e+S)-\left[D_e\sinh x_o+SL_e\cosh x_o+\alpha L_e(SL_e\sinh x_o+D_e\cosh x_o)\right]e^{-\alpha x_j}\right\}\left\{n_o D_e(D_e\sinh x_o+SL_e\cosh x_o)+\frac{p_o D_h L_e(SL_e\sinh x_o+D_e\cosh x_o)}{\frac{(x_t-x_j)}{L_h}\tanh\frac{(x_t-x_j)}{L_h}}\right\}^{\frac{1}{2}}}{2(\alpha^2L_e^2-1)\left\{n_o(SL_e\cosh x_o+D_e\sinh x_o)+\frac{p_o L_e D_h(SL_e\sinh x_o+D_e\cosh x_o)}{L_H D_e\tanh\frac{(x_t-x_j)}{L_h}}\right\}\left\{L_e(SL_e\sinh x_o+D_e\cosh x_o)\right\}^{\frac{1}{2}}} . \tag{32}$$

An attempt will be made to compute numerically these equations by means of a computer analysis. The results would then be available in graphical form.

C. ARRAY FABRICATION

1. Mesa Array

Single etched mesa devices were used early in the program, to evaluate both diffusions and etches. Devices were made by masking a diffused wafer with a soluble wax and etching. The wafer was usually bonded with indium to a gold-clad header and a gold wire was indium-soldered to the top of the mesa.

Experiments with etches showed that a mixture (by vol.) in 12 HNO_3, 4HF, and H_2O followed by a flowing rinse in H_2O_2, which has been used by others in this field, works quite well. Other InAs etches tend to leave a surface residue at the junction which electrically acts as a shunting resistor.

The etching techniques were then combined with masking technology to fabricate mesa arrays (see Figure 4). A diffused wafer was etched to remove 5 microns of p-region and then coated with centrifuged and diluted HPR resist. The pattern is then formed in the resist by standard processes leaving mesas of HPR on 0.005" centers. The structure is then etched to a depth greater than the remaining 15 μ of p-region and the mask is removed by stripping. A pattern of contact pads of cadmium-gold can be formed by evaporation or photoresist-etch techniques prior to the mesa etch photoresist step; this technology will be discussed in the section on lead attachment.

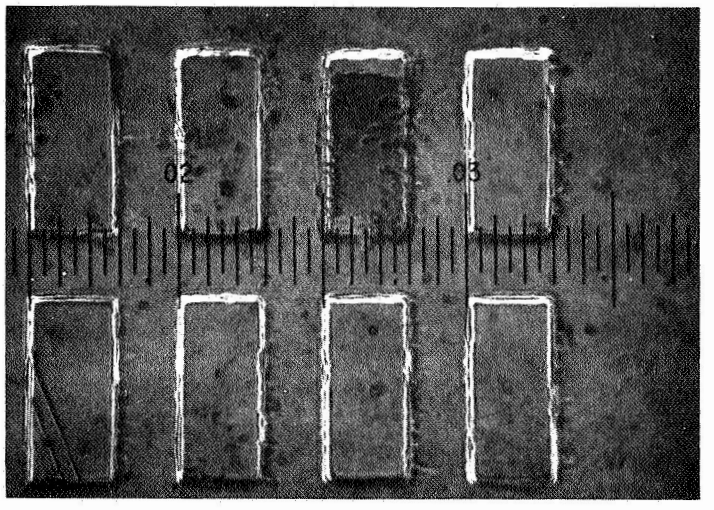


Figure 4. Etched Mesa Photodiode Array

Several difficulties have been noted with the mesa process. The photoresist adherence is not adequate for deep etching with uniform edges due to under cutting and the resultant loss of straight-line edge definition of the mesas. This is directly attributed to the vigor of the etchant and the degree of adherence of the photoresist. Diluting the etch with additional H_2O causes a residue to form on the junction edge of the mesas. Furthermore, lead attachment for batch fabrication of the electroded arrays is severely complicated by the mesa edge step. For these reasons, the mesa array approach was not continued.

2. Planar Array

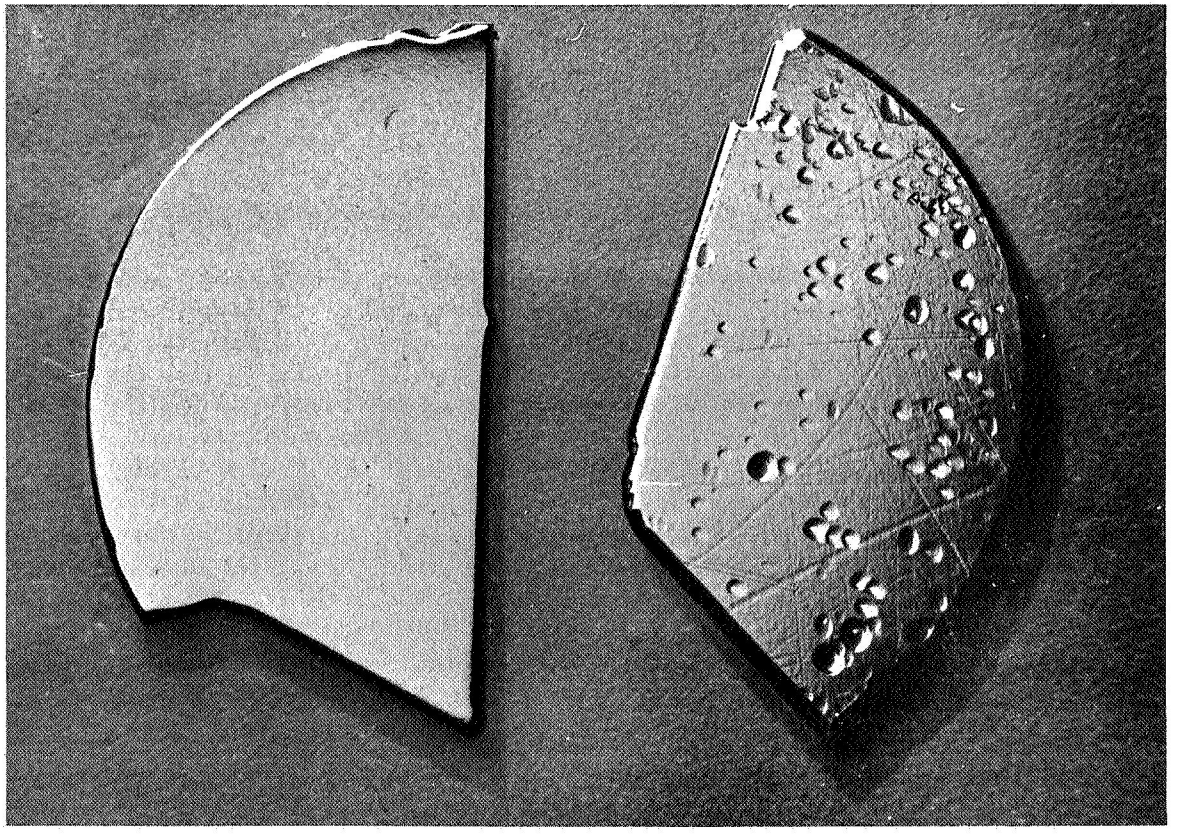
Indium arsenide arrays were also fabricated by the planar technique. Two reasons for this approach were: (1) greater density due to higher resolution from the photoresist process and (2) compatibility with lead attachment.

The planar indium arsenide array was prepared with the following steps:

a) Material preparation
b) SiO_2 masking and array pattern etching
c) Diffusion of planar array
d) Post-diffusion wafer preparation for leads
e) Lead attachment

a. Material Preparation

The present material for the array is indium arsenide, N-type, with a carrier concentration of 2.9×10^{16} and a bulk resistivity of 0.070 ohm-cm. The InAs boule is mounted and sliced parallel to the B-face. After slicing, the wafers are demounted and cleaned. The A and then the B-face of the wafers are lapped parallel and the B-face is mounted so that it can be optically and chemically polished. The B-face is polished to a highly reflective-scratch-free surface using 0.3μ alumina and a 1% bromine – 99% methanol chemical polish. This final step removes all surface damage from 0.3μ alumina polishing and leaves a scratch-free, optically flat B-face. After polishing, the wafer is removed from the holder, cleaned and stored in an evacuated dessicator until needed for array processing. The effect of the bromine-methanol etch is illustrated in Figure 5.



B-Face Arsenic A-Face Indium

Figure 5. Face After Chemical Polishing

b. SiO_2 Masking and Array Pattern Etching

This part of the planar array processing is prepared in two steps: (1) Surface cleaning and oxide masking and (2) HPR process and etching array pattern.

(1) Surface Cleaning and Oxide Masking. The InAs wafer is removed from storage, diced into the prescribed geometry, and cleaned. Cleaning consists of immersion in boiling trichloroethylene, followed by propanol vapor to remove all water-soluble surface contaminants. It is then dipped in concentrated hydrofluoric acid for five seconds, rinsed in propanol, and blown dry. At this point, the wafer is pre-oxidized in an oxygen atmosphere at 500°C for 10 minutes, with an O_2 flow rate of 150 cc/minute. This is done to form an oxide interface between the SiO_2 passivation layer and the InAs surface. This step creates a very strong bond between the InAs and the SiO_2. The pre-oxidized wafer is then placed in the glow discharge deposition chamber for SiO_2 masking.[1, 2]

(2) HPR Process and Etching Array Pattern. Following SiO_2 deposition, the sample is removed from the chamber and coated with homogenized photoresist, air dried at room temperature and pre-baked at 80°C. The coated wafer is exposed, developed, and post-baked for one hour at 150°C. The wafer is then etched with ammonium bi-flouride until all the unprotected SiO_2 windows are etched away. The HPR is removed by ultrasonic agitation in xylene. This removal is enhanced by a 30-minute storage in a 10^{-6} torr vacuum chamber prior to the ultrasonic stripping. Figure 6 shows the 5×7 mil windows etched in an SiO_2 coated wafer. Figure 7 shows a side view of the masked array prior to diffusion.

c. Diffusion of Planar Array

The diffusion of the SiO_2 planar array is performed in two steps.

(1) Ampule and Wafer Preparation. A one-centimeter O.D. quartz tube, 8 inches long, is first etched with acid etch 41 for one hour. After this etching, the tube is thoroughly rinsed with de-ionized-distilled water, and filled with aqua-regia to soak for $\frac{1}{2}$ hour. These two steps remove the surface impurities on the inside diameters of the quartz tube.

[1] "Glow Discharge Formation of Silicon Oxide and the Deposition of Silicon Oxide Thin Film Capacitors by Glow Discharge Technique," by Ing and Davern, Journal of Electrochemical Society, Vol. 112, No. 3, March 1965.

[2] "Use of Low Temperature Deposited Silicon Dioxide Films as Diffusion Mask in GaAs," by Ing and Davern, Journal of Electrochemical Society, January 1964.

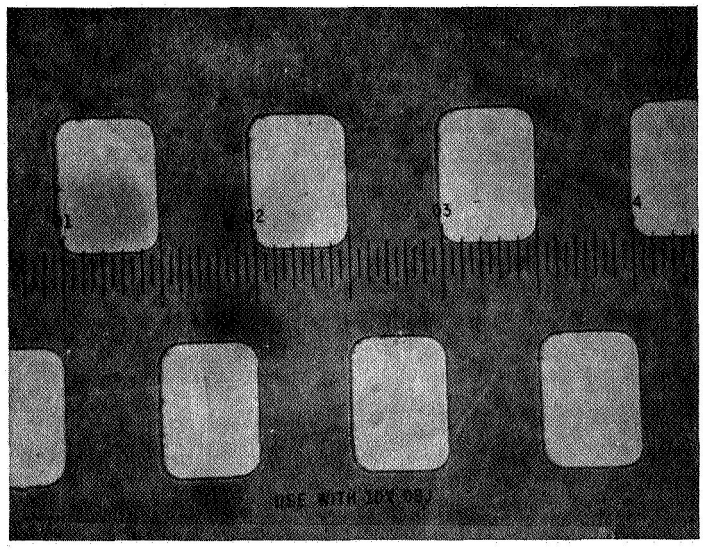


Figure 6. SiO_2 Masked Planar Array

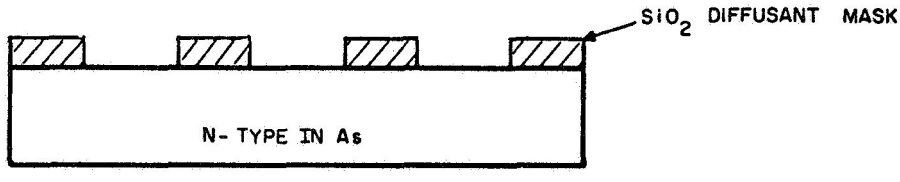


Figure 7. Side View of SiO_2 Masked Planar Array

After the aqua-regia, the tube is rinsed with de-ionized distilled water followed by high-purity propanol. The tube is then evacuated to 7×10^{-7} torr over a liquid nitrogen cold trap and flamed out up to $800^{o}C$ to drive off impurities that may still be present on the quartz walls. The tube is then cooled to room temperature, vacuum broken and charged with the dopants and wafers. The ampule with charge is shown in Figure 8.

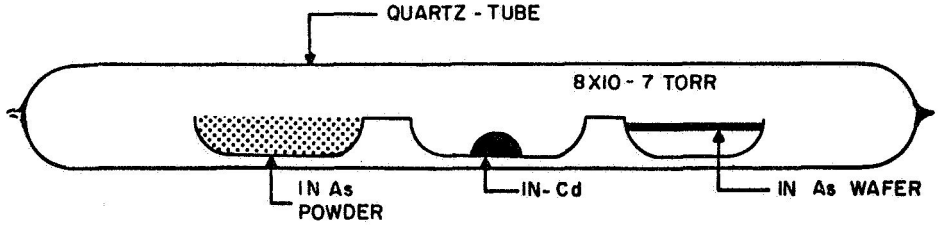


Figure 8. Ampule with Charge

(2) Diffusion. After the quartz tube is charged with the dopant, wafer and indium arsenide powder, it is sealed off to a vacuum of 8×10^{-7} torr. The indium arsenide powder is placed in the ampule to keep the arsenic vapor pressure high, so the wafer to be diffused will not become pitted. The dopant source is an alloy of 17.5 mg of indium plus 2.5 mg of cadmium and is prepared just prior to the diffusion run. A diluted source is used in order to prevent "epi" growths on the indium arsenide wafer. A small quartz boat shown in Figure 8 is used to hold the diffusion materials, preventing the materials from moving around in the tube during seal-off and causing surface contamination between the diffusion materials. The diffusion cycle is performed at 740°C for a total time of 21 minutes. It requires 13 minutes for the furnace to recover to 740°C, thus the diffusion time at the 740°C temperature is 8 minutes. The diffusion ampule is then air-quenched and the diffused wafer is removed. The wafer then appears as shown in Figure 9.

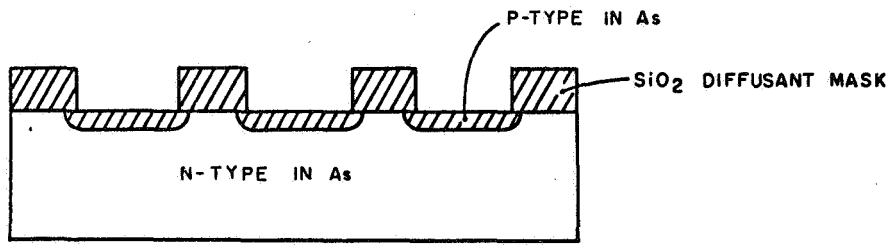


Figure 9. Diffused Planar Array

d. Post Diffusion Wafer Preparation for Leads

After diffusion, the SiO_2 diffusant masking is removed by immersing the wafer in hydroflouric acid for ten seconds, then rinsing the wafer's surface with distilled water. The planar diffused wafer surface is etched for one second in a freshly prepared etchant of 12 parts concentrated nitric acid, 4 parts concentrated hydroflouric acid, and one part distilled water. Immediately after etching the wafer is placed in a 30% hydrogen peroxide solution and then rinsed with distrilled water. This etch removes approximately 5 microns of the N and P region, reducing surface contamination which can cause lateral conduction or shunting between the N and P regions on the planar surface. This step is illustrated in Figure 10.

e. Lead Attachment on Planar Array

After diffusion and surface etching, the clean planar array is again coated with HPR. Windows are open in the p-region of the diode for metallic contact and passivation of the rest of the InAs surface. As shown in Figure 11, this step also leaves approximately a $\frac{1}{2}$ mil HPR overlap on the perimeter of the rectangular p-region in order to prevent shorting of the P-N edge of the junctions by the metallic Ni-Cr + Au lead.

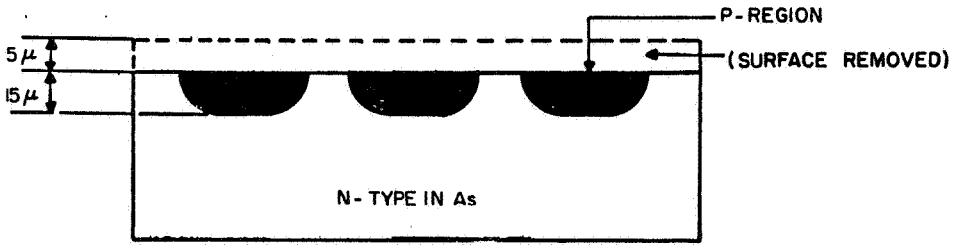


Figure 10. Stripped Diffused Planar Array

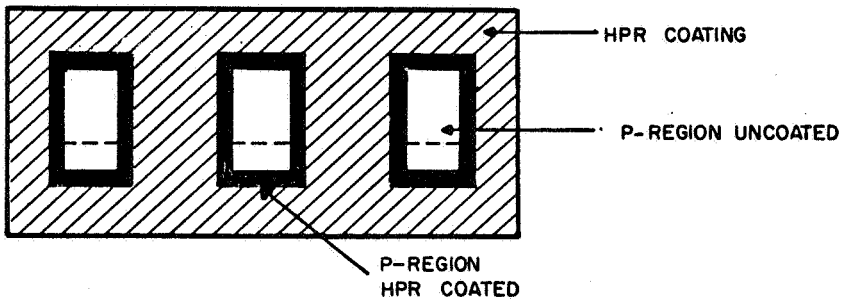


Figure 11. HPR Coated Diffused Planar Array

The wafer is then vacuum-coated with successive layers of Ni-Cr and gold. The nichrome film is deposited to a resistivity of 1×10^8 ohms/sq. and the gold is deposited to a resistivity of 2 ohms/sq. After metallic deposition, the substrate is coated with Shipley A-Z resist and cured. It is then exposed for 2 3/4 minutes, using a positive mask for the lead pattern. The leads are formed by etching the Ni-Cr+Au unprotected regions by using "Lea-Ronal" Gold Stripper. This requires about one minute. The A-Z photoresist that remains on the Ni-Cr+Au lead pattern is then removed, and the planar array is ready for lead contact to the external circuitry.

The electrode configurations are detailed in Figures 12a and b. A complete array is shown in Figure 13.

D. DEVICE AND ARRAY OPERATION

The initial series of diode arrays contained fifty elements with a resolution of 200 elements/inch. Each array was checked under saturated light conditions. If reasonable response was obtained from randomly checked elements, the array was mounted to a fixture and D* detectivity was measured. Array diodes generated approximately 2 mv under saturated light conditions. The D* mean average of these arrays was 3.2×10^8 at $200^{\circ}K$.

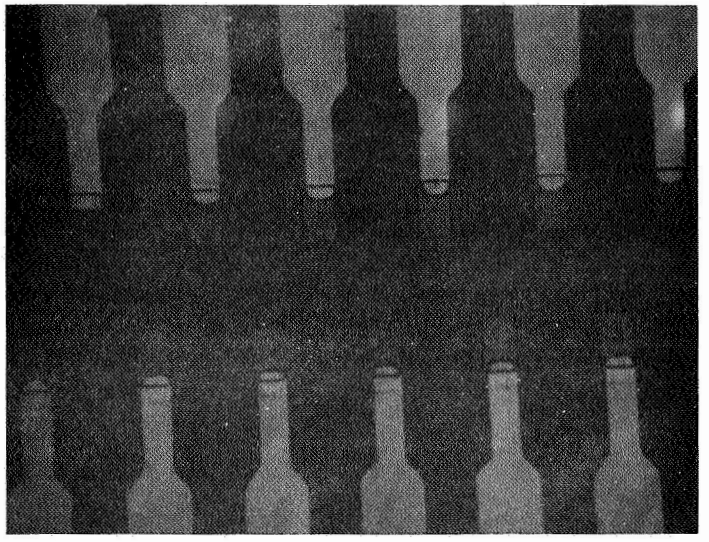


Figure 12a. Finished Planar Array with Leads

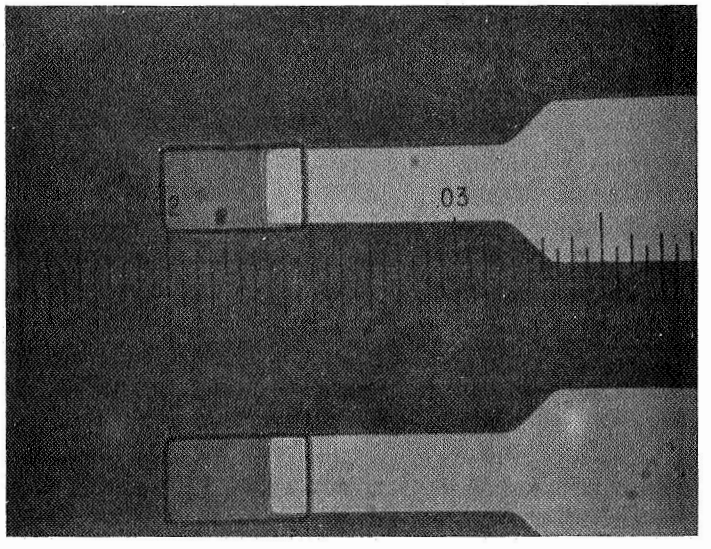


Figure 12b. Enlargement of Detector Area

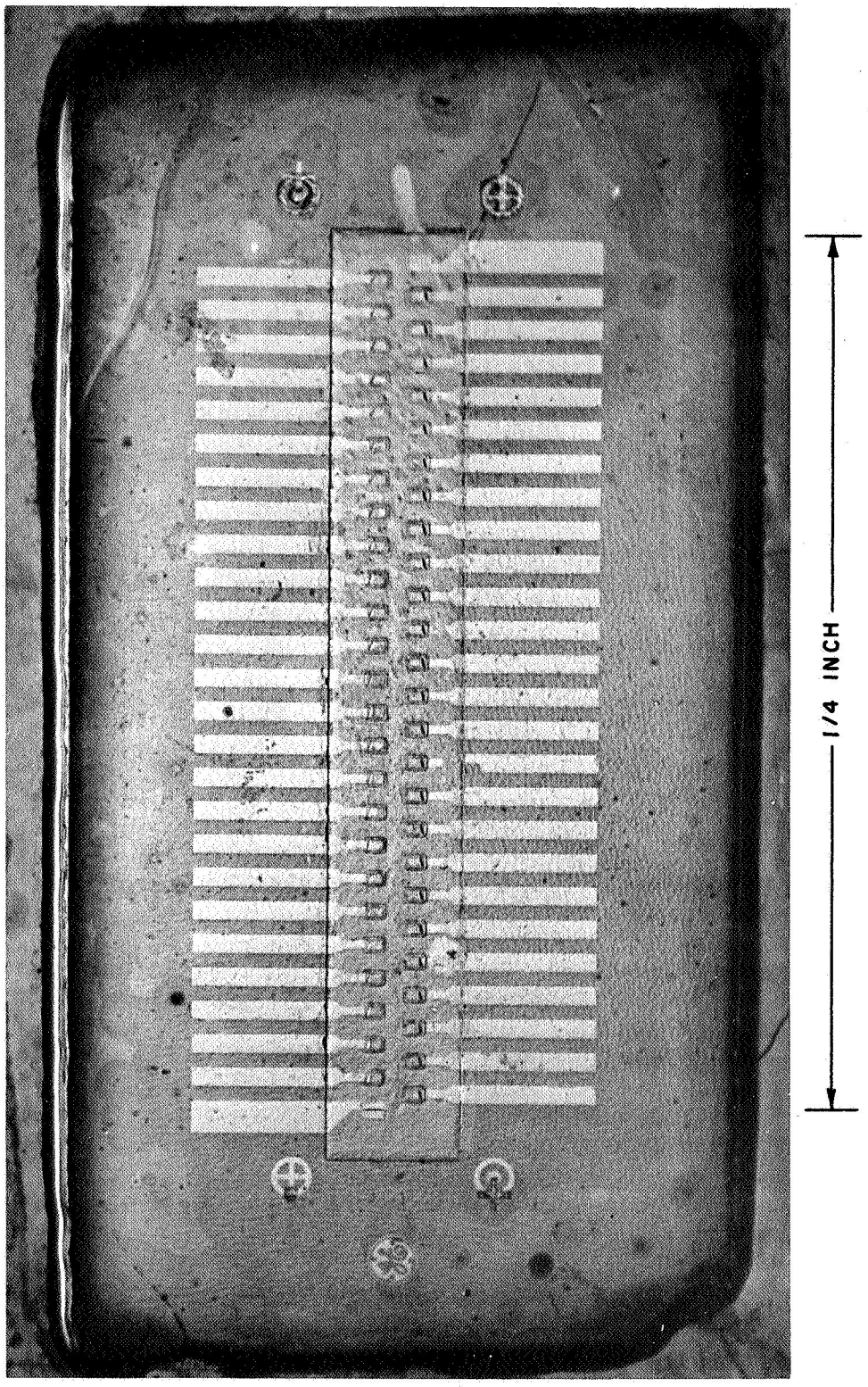


Figure 13. Fifty-element InAs Detector Array

During the second half of the array development program, the mask set and processes described in Section II.C. were utilized to fabricate the diode arrays. Testing of these arrays again consisted of spot checks under saturated light conditions, using microprobes. Cooling was obtained from a cold nitrogen gas jet directed onto the surface of the wafer. Frost formation was not appreciable during the first 10-12 minutes of cooled operation, allowing adequate time for probing. Photovoltages measured under these conditions were typically 2-4 millivolts.

Arrays were then packaged in the custom package described in Section III.B. of this report. All subsequent tests were therefore carried out on the total circuit, consisting of the printed-circuit board, the thin-film electrode from the PC board to the diode lead, the diode-array electrode, and the diode. The lens, shown in Figure 23, is uncoated "IRTRAN"-2.

After packaging, each array was checked for continuity to the external circuit connectors at 300°K and at 200°K. As noted in Section III.C., some leads did fail or become discontinuous upon cooling. Therefore, in the following data, some detectivity measurements are not listed on the computer analysis data sheet. Each detector array was measured under the following conditions:

Blackbody Temperature	=	843°K or 570°C
Array Temperature	=	-75°C
Distance B.B. to Array	=	7.0 inches
Noise Bandwidth	=	6.0 Hz
Diameter of B.B. Aperture	=	0.05 inches
System Gain	=	2000
Area of Detector	=	0.105E-04 square inches

RMS values of signal and noise voltages were recorded. Data was subsequently fed into a computer for calculation
through IV show the computer print-out of array operation. Each table lists only those diodes that have leads on the same side of the array (see Figure 13).

The best operation was obtained from Array B5L. From Table IV, the following data are obtained, based on the 23 out of 25 accessible diodes:

$$\text{Max } D^*_{bb} = 6.19 \times 10^{10}$$
$$\text{Min } D^*_{bb} = 2.24 \times 10^{9}$$
$$\text{Ave } D^*_{bb} = 1.03 \times 10^{10}$$
$$\text{Median } D^*_{bb} = 4.57 \times 10^{9}$$

where D^*_{bb} is obtained by measurements with a black body source. The number of diodes within a given spread of the median D^*_{bb} is indicated in the following data.

Within ± 20% ----- 7 devices (31%)
Within ± 30% ----- 14 devices (62%)
Within ± 50% ----- 16 devices (70%)
Within ± 100% ---- 19 devices (83%)

TABLE I

OPTICAL RESPONSE ARRAY B1L – RIGHT

ARRAY EL.	RMS SIGNAL VOLTAGE	RMS NOISE VOLTAGE	D* DETECTIVITY	RESPONSIVITY
1	28.000MV	.300MV	7.612E+08	5.476E+03
2	30.000MV	.300MV	8.155E+08	5.867E+03
3				
4	28.000MV	.500MV	4.567E+08	5.476E+03
5	26.000MV	.600MV	3.533E+08	5.085E+03
6	23.000MV	.800MV	2.343E+08	4.498E+03
7	27.000MV	1.000MV	2.201E+08	5.280E+03
8	21.000MV	1.000MV	1.711E+08	4.107E+03
9	19.000MV	1.000MV	1.547E+08	3.716E+03
10				
11	20.000MV	1.500MV	1.084E+08	3.911E+03
12	21.000MV	3.100MV	5.464E+07	4.107E+03
13				
14				
15				
16				
17				
18	20.000MV	1.000MV	1.629E+08	3.911E+03
19	20.000MV	1.000MV	1.629E+08	3.911E+03
20	20.000MV	1.500MV	1.084E+08	3.911E+03
21	20.000MV	1.500MV	1.084E+08	3.911E+03
22	20.000MV	1.500MV	1.084E+08	3.911E+03
23	52.000MV	1.000MV	4.240E+08	1.017E+04
24	52.000MV	1.000MV	4.240E+08	1.017E+04
25	48.000MV	1.300MV	3.010E+08	9.387E+03
MEANS	19.800MV	.796MV	2.052E+08	3.872E+03

TABLE II

OPTICAL RESPONSE ARRAY B4L - LEFT

ARRAY EL.	RMS SIGNAL VOLTAGE	RMS NOISE VOLTAGE	D* DETECTIVITY	RESPONSIVITY
1				
2				
3				
4				
5				
6	60.000MV	1.000MV	4.893E+08	1.173E+04
7	6.000MV	.500MV	9.753E+07	1.173E+03
8	40.000MV	.400MV	8.155E+08	7.823E+03
9	21.000MV	1.500MV	1.139E+08	4.107E+03
10	28.000MV	.400MV	5.709E+08	5.476E+03
11	22.000MV	.450MV	3.986E+08	4.302E+03
12				
13	6.800MV	.450MV	1.230E+08	1.330E+03
14				
15				
16				
17				
18	6.500MV	.400MV	1.323E+08	1.271E+03
19	2.000MV	.350MV	4.589E+07	3.911E+02
20	70.000MV	.350MV	1.631E+09	1.369E+04
21	66.000MV	.350MV	1.538E+09	1.291E+04
22				
23	18.000MV	.500MV	2.935E+08	3.520E+03
24	18.000MV	.400MV	3.669E+08	3.520E+03
25	160.000MV	.500MV	2.610E+09	3.129E+04
MEANS	20.972MV	.302MV	3.691E+08	4.101E+03

TABLE III

OPTICAL RESPONSE ARRAY B4L – RIGHT

ARRAY EL.	RMS SIGNAL VOLTAGE	RMS NOISE VOLTAGE	D* DETECTIVITY	RESPONSIVITY
1				
2	150.000MV	.400MV	3.058E+09	2.933E+04
3	22.000MV	.400MV	4.485E+08	4.302E+03
4	22.000MV	.450MV	3.986E+08	4.302E+03
5	2.500MV	.300MV	6.747E+07	4.889E+02
6	50.000MV	1.000MV	4.077E+08	9.778E+03
7	17.000MV	.800MV	1.731E+08	3.325E+03
8	5.500MV	.350MV	1.279E+08	1.076E+03
9	50.000MV	.400MV	1.019E+09	9.778E+03
10	110.000MV	.300MV	2.990E+09	2.151E+04
11	130.000MV	.400MV	2.651E+09	2.542E+04
12	64.000MV	.300MV	1.740E+09	1.252E+04
13	54.000MV	.300MV	1.468E+09	1.056E+04
14	7.000MV	.400MV	1.425E+08	1.369E+03
15	135.000MV	.400MV	2.753E+09	2.640E+04
16	52.000MV	.400MV	1.060E+09	1.017E+04
17	190.000MV	.350MV	4.427E+09	3.716E+04
18	100.000MV	.400MV	2.039E+09	1.956E+04
19	50.000MV	.400MV	1.019E+09	9.778E+03
20	140.000MV	.500MV	2.284E+09	2.738E+04
21	275.000MV	.400MV	5.607E+09	5.378E+04
22	76.000MV	.400MV	1.550E+09	1.486E+04
23	160.000MV	.450MV	2.900E+09	3.129E+04
24				
25				
MEANS	74.480MV	.380MV	1.533E+09	1.457E+04

TABLE IV

OPTICAL RESPONSE ARRAY B5L – LEFT

ARRAY EL.	RMS SIGNAL VOLTAGE	RMS NOISE VOLTAGE	D* DETECTIVITY	RESPONSIVITY
1	280.000MV	.300MV	7.612E+09	5.476E+04
2	4000.000MV	1.500MV	2.175E+10	7.823E+05
3	3800.000MV	.500MV	6.198E+10	7.432E+05
4	3800.000MV	.750MV	4.132E+10	7.432E+05
5	1600.000MV	.500MV	2.610E+10	3.129E+05
6				
7	1300.000MV	1.500MV	7.068E+09	2.542E+05
8				
9	460.000MV	1.000MV	3.752E+09	8.996E+04
10	460.000MV	1.300MV	2.886E+09	8.996E+04
11	460.000MV	1.300MV	2.886E+09	8.996E+04
12	440.000MV	1.600MV	2.243E+09	8.605E+04
13	460.000MV	1.000MV	3.752E+09	8.996E+04
14	430.000MV	1.000MV	3.507E+09	8.409E+04
15	450.000MV	.800MV	4.588E+09	8.800E+04
16	440.000MV	1.000MV	3.589E+09	8.605E+04
17	420.000MV	1.000MV	3.425E+09	8.214E+04
18	410.000MV	.750MV	4.459E+09	8.018E+04
19	420.000MV	.750MV	4.567E+09	8.214E+04
20	380.000MV	.600MV	5.165E+09	7.432E+04
21	420.000MV	.600MV	5.709E+09	8.214E+04
22	360.000MV	.500MV	5.872E+09	7.040E+04
23	340.000MV	.500MV	5.546E+09	6.649E+04
24	230.000MV	.400MV	4.690E+09	4.498E+04
25	180.000MV	.400MV	3.670E+09	3.520E+04

III. ARRAY MODULE

A. INTRODUCTION

Incorporating the diffused and electroded array of Figure 13 into an electronically scanned system requires a set of interconnecting leads from each diode to its associated preamplifier and commutator terminal. Any such leads must be able to make good electrical contact to the NiCr+Au leads on the InAs chip, as well as provide fan-out to the external circuitry. Since the array is cooled and therefore operates as a dewar, vacuum feed-throughs must also be provided.

Flying leads between the wafer and glass-sealed vacuum feed-through pins are one approach, although many problems exist with this technique. A significant problem that occurs with the array fabrication process that was utilized is the limited temperature to which the InAs wafer can be subjected as a result of the organic isolation layer. The modified KMER used as a surface protection for the thin-film leads is limited, in temperature, to 150-170°C. Thus, any wire bonding would necessarily have to be either low-temperature soldering, welded wire, or ultrasonic bonding. However, adherence to the NiCr+Au lead on the SiO_2 over InAs was found to be critical and further techniques were evaluated.

Most desirable of the alternative approaches is the use of thin-film leads over the edge of the chip. This approach is definitely more advantageous for the final operational model of any solid-state image sensor array, since reliability and ruggedness are increased through the elimination of flying leads.

B. MOLDED BLOCK DIAGRAM

As a result of the -80°C temperature requirement, formation of frost on the InAs array and heat transfer away from the InAs array were the major factors considered in the final design. To eliminate the frost formation problem, a vacuum chamber was required around the InAs array. With the vacuum chamber came the problem of heat transfer and electrical continuity from inside the vacuum chamber to some convenient point outside the chamber. These requirements are met with the design shown schematically in Figure 14.

The main structure is the molded plastic block, which functions as the substrate for the thin-film leads and as a portion of the vacuum enclosure. The block itself was molded from "Isochem-Upox 468" epoxy-urethane. This resin is a polymeric combination epoxy novalac and urethane that provides high tensile shear adhesion and elongation properties plus high impact resistance. The urethane structure incorporated in the epoxy-urethane complex gives added elasticity at low temperatures.

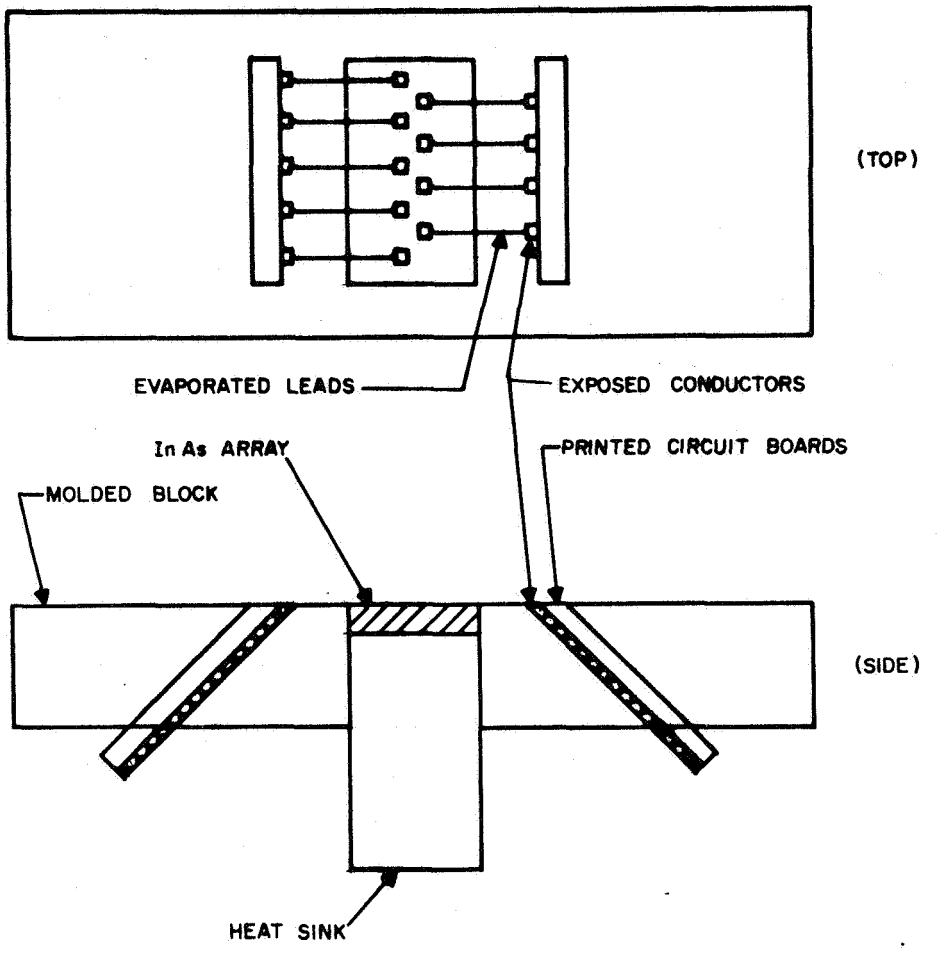


Figure 14. Molded Block Design

The Upox 468 material wets and bonds very well to metal, glass, ceramic, and most semiconductor materials. The fact that it bonds well to itself means that multiple layers can be poured with the previous layer bonding well to the newly-added layer. This is important, since two layers were used in the structure developed for the image sensor array. The top-most surface contains the InAs array and must be polished in order to accept the thin-film lead pattern connecting the printed circuit board leads to the detector lead pattern. This layer contains 50% by weight of silica (quartz) which gives a smooth polishable surface. The second or "bulk" layer contains hollow glass microspheres, 3 to 30 microns in size. The spheres reduce both the thermal conductivity and the thermal expansion of the epoxy. The former is necessary to reduce the heat loss and the resulting cooling source requirements, while the latter is necessary to minimize the differential expansions of the several materials used in the structure. The coefficients of the several materials are listed in Table V.

TABLE V

COEFFICIENTS OF THERMAL EXPANSION OF MATERIALS USED IN IMAGE SENSOR MODULES

Material	$\Delta L/L/^{o}C \times 10^{-6}$ ($-100^{o}C$ - $25^{o}C$)
Indium Arsenide	4
Copper	15
Textolite Block	15 to 20
Printed Circuit Board	12 to 15
Upox 468 S(50μ silica filled)	25 to 30
Upox 468 (microsphere filled)	25 to 30

A photograph of the molded block is shown in Figure 15.

C. COOLED OPERATION

The arrays were tested for continuity, both before and after cooling to $-80^{o}C$. The results of the testing are shown in Tables VI through XI. The photograph of Figure 16 shows the location of the discontinuity in the thin-film leads. On arrays that were re-metalized following cooling, continuity was regained. However, subsequent cooling caused the discontinuity to reappear, in the same location.

Elimination of this problem is directly related to the thermal mismatch of the several materials used in the construction of the block. Improvements are possible in the expansion coefficients of both the heat sink and the epoxy. The heat sink expansion coefficient can be reduced from the 16×10^{-6} of copper to 4×10^{-6} with Kovar, while the epoxy material expansion coefficient can be further reduced with negative coefficient filters. However, when making a vacuum-tight seal between two materials having a different coefficient of expansion, it is desirable to have the material that leads the thermal gradiant to be the smallest in thermal expansion. By keeping this relationship, the joint is always under compression and this reduces the chance of leakage. Thus, the relationship between the InAs, the heat sink, and the epoxy must be considered in the selection of materials.

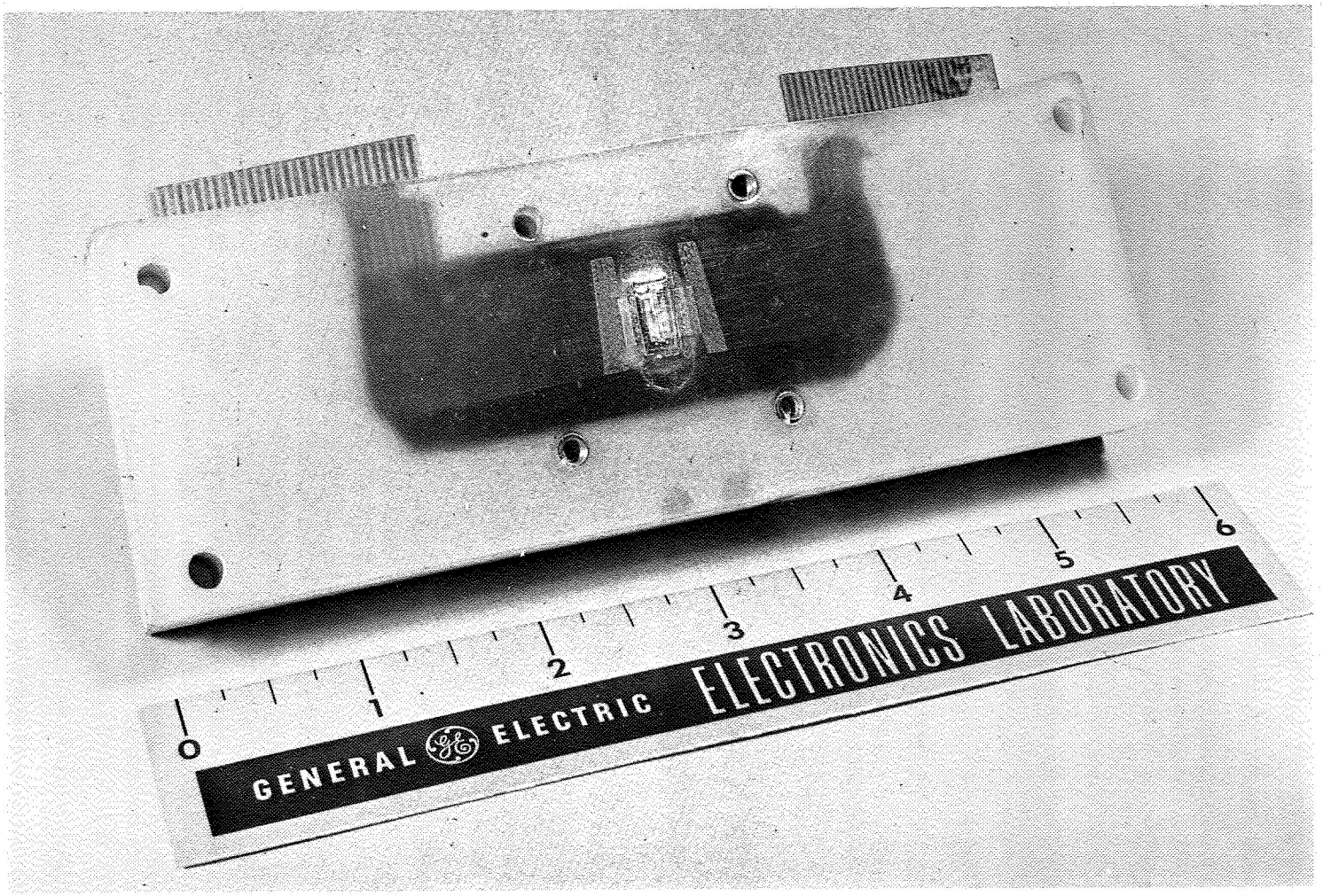


Figure 15. Molded Plastic Block

TABLE VI

COOLING EFFECTS ON ARRAY B3L, LEFT SIDE

(Note: + = continuity; o = open)

No.	Before Cooling	After Cooling to -80°C
1	o	o
2	o	o
3	o	o
4	o	o
5	o	o
6	o	o
7	+	o
8	o	o
9	+	o
10	+	o
11	o	o
12	+	o
13	+	+
14	o	o
15	o	+
16	o	+
17	o	+
18	o	+
19	o	o
20	o	o
21	+	o
22	+	o
23	o	o
24	+	o
25	+	o

TABLE VII

COOLING EFFECTS ON ARRAY B3L, RIGHT SIDE

(Note: + = continuity; o = open)

No.	Before Cooling	After Cooling to -80°C
1	+	+
2	+	+
3	+	o
4	+	o
5	+	o
6	+	+
7	+	+
8	+	+
9	+	+
10	+	o
11	+	+
12	+	+
13	+	+
14	+	o
15	+	o
16	+	+
17	+	+
18	+	+
19	+	o
20	+	+
21	+	o
22	+	o
23	+	+
24	o	o
25	o	o

TABLE VIII

COOLING EFFECTS ON ARRAY B4L, LEFT SIDE

(Note: + = continuity, o = open)

No.	Before Cooling	After Cooling to -80°C
1	+	o
2	+	o
3	+	o
4	+	o
5	+	o
6	+	+
7	+	+
8	+	+
9	+	+
10	+	+
11	+	+
12	+	o
13	+	+
14	+	o
15	+	o
16	+	o
17	+	o
18	+	+
19	+	+
20	+	+
21	+	+
22	+	+
23	+	o
24	+	+
25	+	+

TABLE IX

COOLING EFFECTS ON ARRAY B4L, RIGHT SIDE

(Note: + = continuity, o = open)

No.	Before Cooling	After Cooling to -80°C
1	+	+
2	+	+
3	+	+
4	+	+
5	+	+
6	o	+
7	+	+
8	+	+
9	+	+
10	+	+
11	+	+
12	+	+
13	+	+
14	+	+
15	+	+
16	+	+
17	+	+
18	+	+
19	+	+
20	+	+
21	+	+
22	+	+
23	+	+
24	o	o
25	o	o

TABLE X

COOLING EFFECTS ON ARRAY B5L, LEFT SIDE

(Note: + = continuity; o = open)

No.	Before Cooling	After Cooling to -80°C
1	+	+
2	+	+
3	+	+
4	+	+
5	+	+
6	+	o
7	+	+
8	+	o
9	+	+
10	+	+
11	+	+
12	+	+
13	+	+
14	+	+
15	+	+
16	+	+
17	+	+
18	+	+
19	+	+
20	+	+
21	+	+
22	+	+
23	+	+
24	+	+
25	+	+

TABLE XI

COOLING EFFECTS ON ARRAY B5L, RIGHT SIDE

(Note: + = continuity; o = open)

No.	Before Cooling	After Cooling to 80°C
1	+	+
2	+	o
3	+	+
4	+	+
5	+	o
6	+	o
7	+	o
8	+	o
9	+	o
10	+	o
11	+	o
12	+	o
13	o	o
14	+	+
15	+	o
16	+	+
17	+	+
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20	+	o
21	+	o
22	+	o
23	+	+
24	+	+
25	+	+

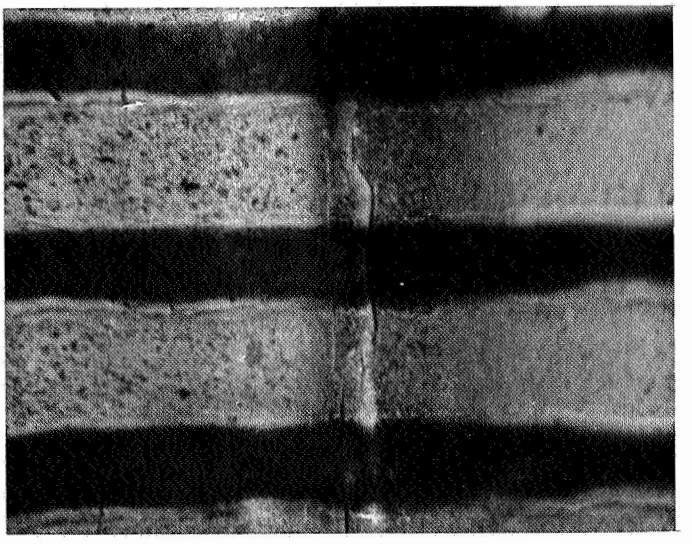

Figure 16. Open Lead After Cooling

IV. SYSTEM DESIGN

The signal processing section of the image sensor array was designed with several central goals centered around compatibility with the detector array in size, operating temperature, and detector characteristics. In addition, practical considerations were considered to realize a working model during the contract period.

The overall system is shown in the system diagram of Figure 17. The system consists of the optical portion before the detectors, including the lens and chopper. Following the detectors are preamplifiers and scanning circuits, with the required supporting scan control circuits and output amplifier circuit. The final signal processing is performed external to the image sensor package, and determines the operating system bandwidth for each detector.

The overall system performance is determined primarily by three factors, the D* of the detector, the noise of the preamplifier, and the system noise bandwidth. Since the latter will be determined external to the scan system, it may be changed at will. The first two are primarily determined by the device (detectors in array or transistors in preamp) and how well they match each other. The system is matched between the detector and preamp such that the effective D* of the system approaches the D* of the detector. In practice,the preamp will add a small amount of noise and the system D* will be slightly lower than the detector D*. The use of the charge storage scanning scheme when used as shown in Fiuure 17 will not greatly alter the system bandwidth. The integration that takes place in the charge storage capacitors is periodically sampled at a rate which is greater than the useful systems bandwidths and hence these externally determined bandwidths will mask the influence of the charge storage scheme.

The preamp has three major functions to perform; (1) stabilize the detector bias, (2) match the detector impedance, and (3) provide power gain. The first consideration of stabilizing the detector bias is a result of using the charge storage technique. The voltage on the charge storage capacitor varies as a function of the incident radiation, integration time, etc. The detector voltage-current characteristic is sensitive to such variations and causes major changes in the performance of the detector. Isolating the detector from the charge storage capacitor with a preamplifier will then allow an independent choice of the optimum detector bias.

The function of impedance matching is the second critical attribute of the preamp. The detector-charge storage combination provides useful results only if an impedance matching transformer is connected between the two elements. Typically, a transformer with an input impedance of 10^5 ohm and an output impedance of greater than 10^9 ohms would be needed to produce the

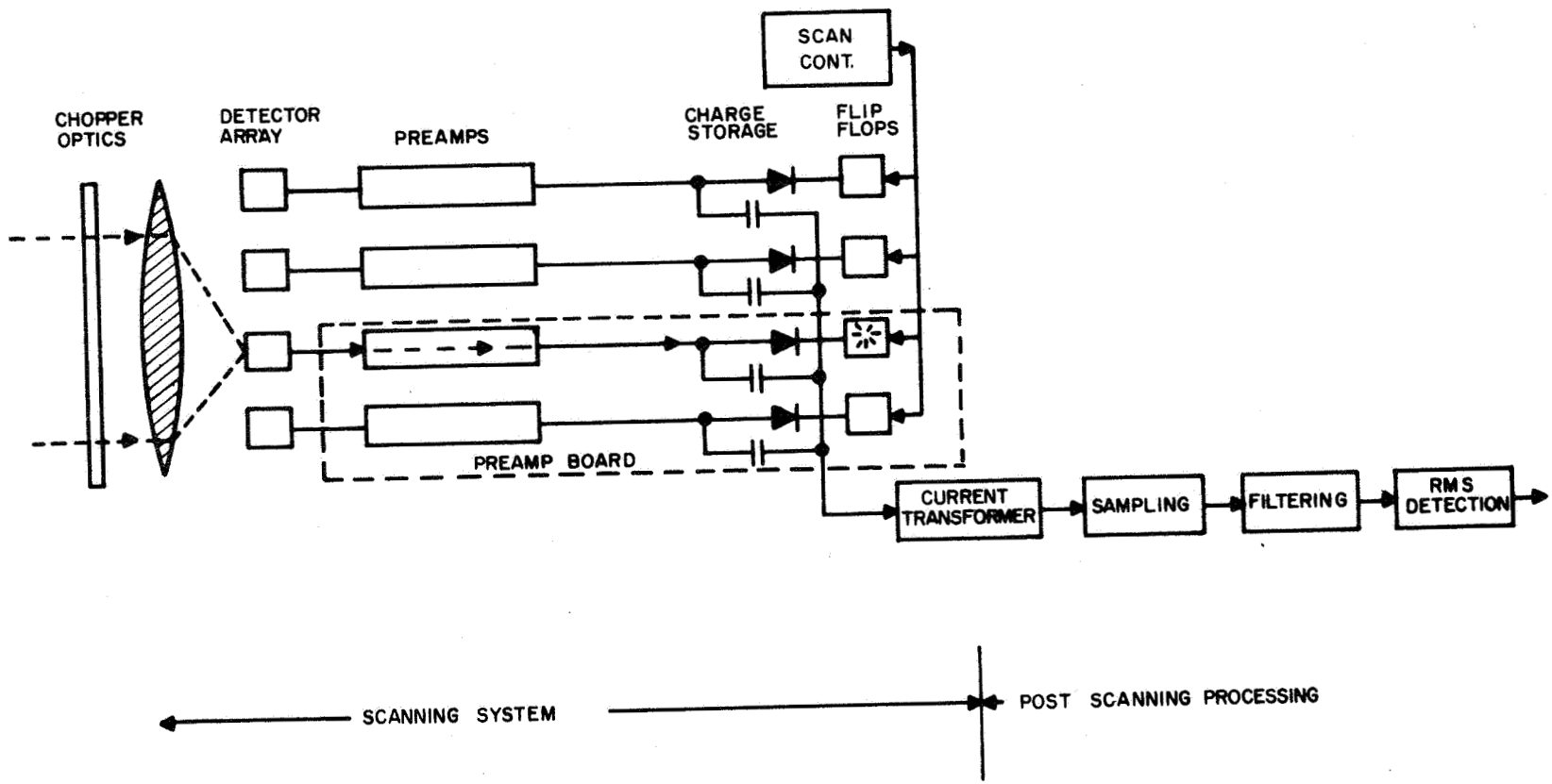

Figure 17. System Operation Diagram

required match. The desired use of microelectronic circuitry and the exceedingly large impedance ratios required for the transformer dictate the use of a preamplifier between each detector and its charge storage capacitor.

The input impedance to the preamplifier was based on the optimization of the system noise, power transfer, and detector performance. In general, these requirements conflict, and a compromise was made. The design chosen also took into account the range of values obtainable with preamp input components. Impedance matching with respect to noise will produce the best system D* and is a prime consideration. Impedance matching with respect to maximum power transfer results in the lowest required power gain of the preamp and hence the fewest components. However, the latter optimum impedance value will not be significantly more efficient than the value chosen for the best noise characteristics.

Preamps using low-noise bipolar transistors offer the following advantages: the bipolar transistors are at a more advanced level of technology, particularly in integrated arrays; they occupy 1/3 to 1/5 the area of J-FETS (Junction Field Effect Transistors); they can have a low noise at some impedance level, and this usually matches the detector impedance reasonably well; and bipolar transistors can operate with 1/10 to 1/100 of the current at which a J-FET operates and have a corresponding lower power dissipation.

The following described circuit is shown in Figure 18. The circuit design includes two complete preamplifiers and their respective charge storage capacitors, as well as the scanning circuitry associated with these preamps. For purposes of explanation, only the left-side preamp will be considered.

The detector is connected to the base of differential transistors Q_1. R_2 is constant current source resistor for Q_1, while R_3 and R_4 are load resistors for Q_1. Inputs to the second stage differential pair, Q_2, are taken from the Q_1 collectors. The differential pair is operated from a constant current source through R_1. The voltage across R_9 follows the detector voltage by virtue of the negative feedback.

The use of complementary transistors in the second state also allows dc negative feedback for bias stabilization. The negative feedback resistor is R_9. The degree of balance to eliminate saturation of the charge storage capacitor (C_1) is compensated by resistor R_{11}.

In summary, the design goals of the preamp are (1) ultimate integration, (2) minimum size/component count per preamp, (3) low noise figure, (4) low temperature operation, and (5) matched system impedances. A photograph of the preamp board is shown in Figure 19.

Read-out of the scanning system is accomplished by sampling the voltage across the charge storage capacitors with the outputs from a flip flop, the SN7474 shown in the circuit diagram. The charging current is passed through a current transformer to the post scanning process indicated in Figure 17. At this point, the signals are sequential, with a one-microsecond pulse width and a 1.25-millisecond period. Two samples are taken during this period, one in the light and one under dark conditions. This is accomplished with the 800 cps chopper placed in front of the array.

The post processing consists of sampling the periodic light and dark readings from a single channel and passing this signal through a narrow-band filter. The resulting RMS voltage is a measure of the signal-to-noise ratio of that particular detector element.

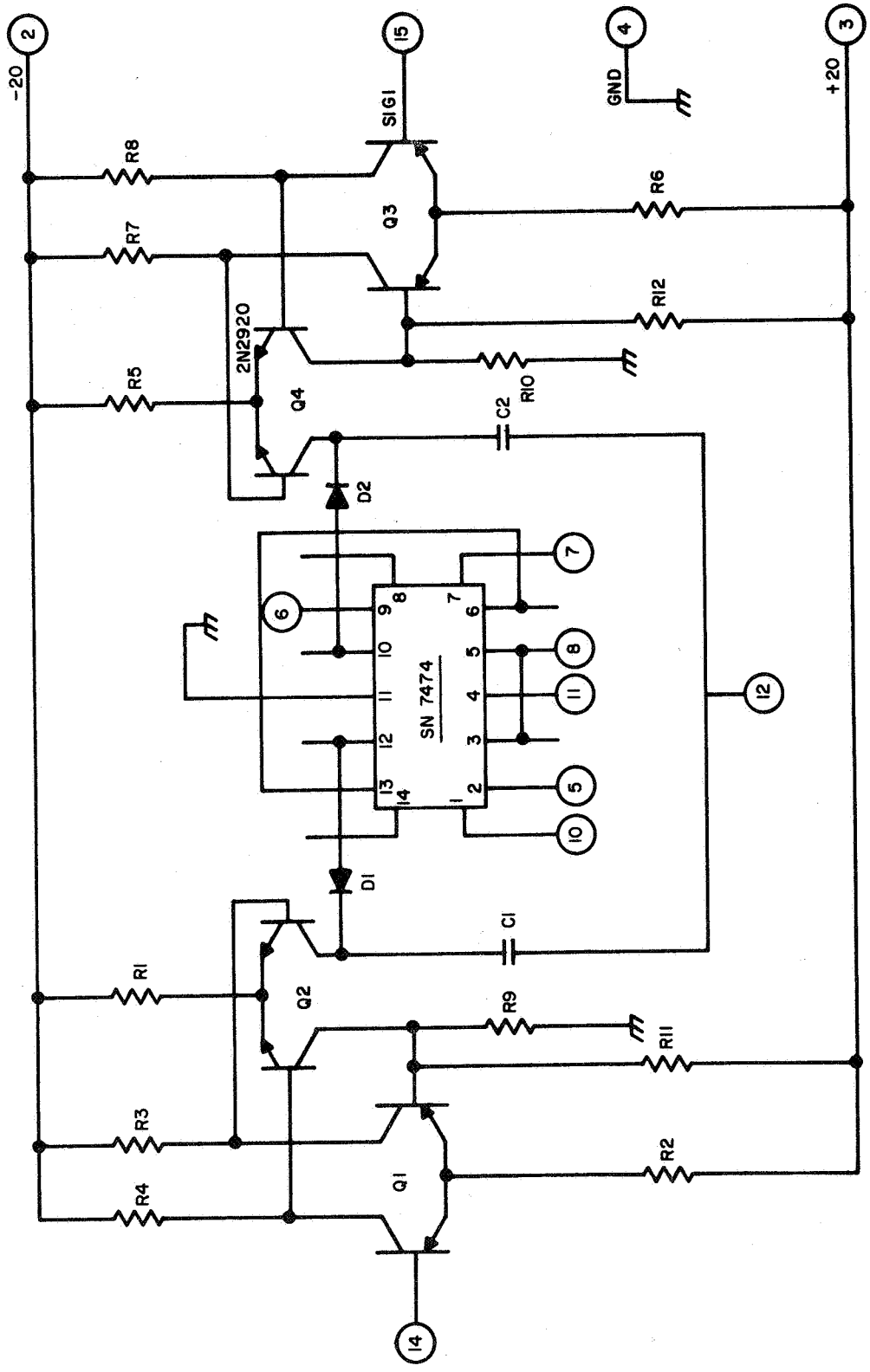

Figure 18. Dual Preamplifier Circuit Board

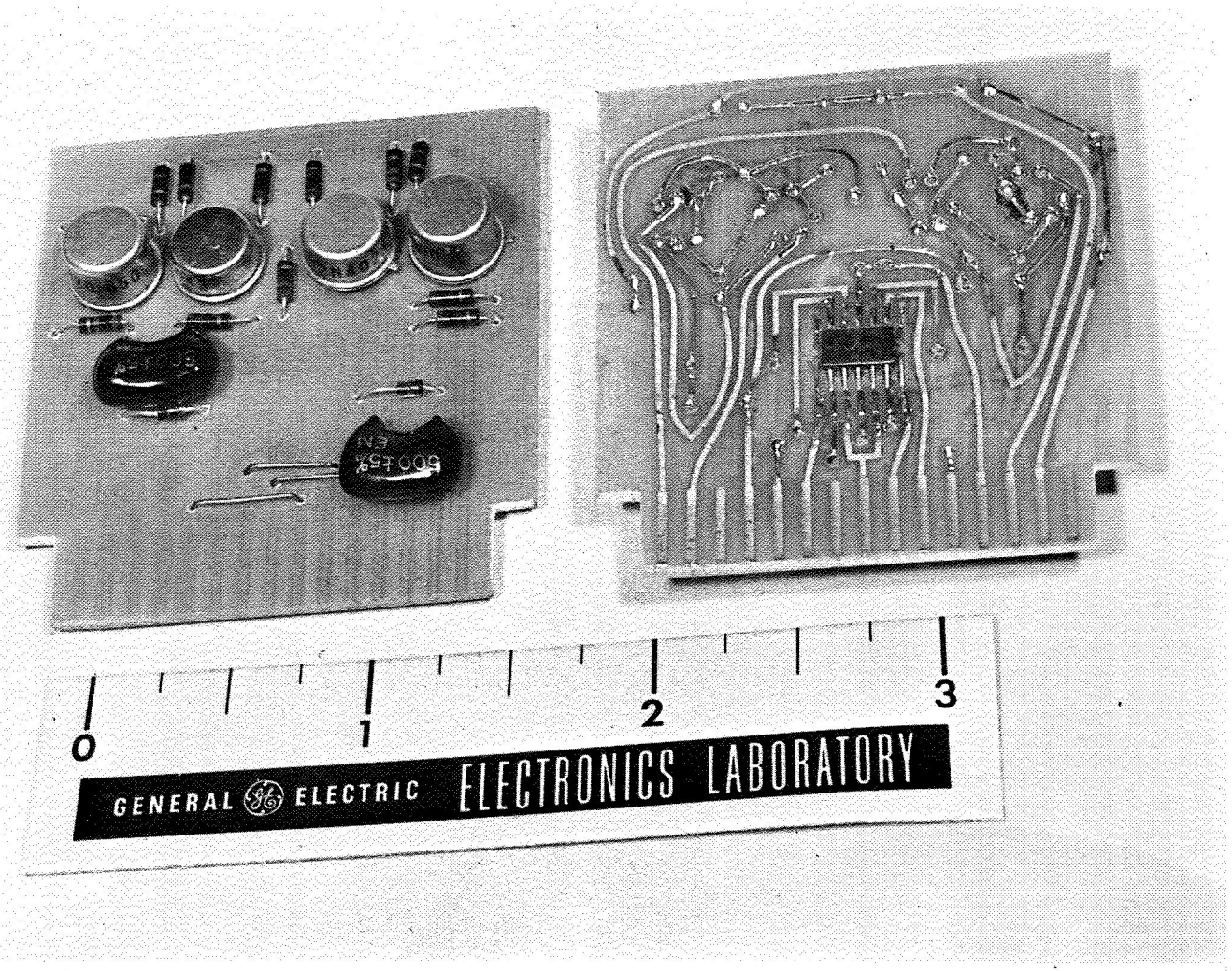

Figure 19. Preamplifier Board

V. ASSEMBLED MODEL

The complete IR detector system is shown in Figure 20. The prime unit in the system is the detector camera, containing the sensor head and associated preamplifier circuitry. The detector camera is mounted on a dewar containing liquid nitrogen that is used to obtain the cryogenic operating temperature at the diode array. An auxiliary chassis provides DC power and secondary circuit functions for the IR camera as well as fine temperature control for the array. Approximate weights and the sizes of each unit are as follows:

	Wt. (lbs)	Height	Length	Width
Detector camera	7 1/4	6.38	12.50	4.00
Dewar (less nitrogen)	4 1/4	3.62	12.05	8.00
Auxiliary chassis	5 1/2	4.00	7.50	8.00

A. PACKAGE DESIGN

1. Detector Camera

The detector camera package is designed about the molded plastic block containing the diode array (Figure 15) since this is the heart of the system. The block is 2" wide by 5-7/8" high by 7/8" thick and camera dimensions are closely related to block gemoetry. The camera is designed to be as small and portable as possible, but no special or costly attempt at miniaturization was made for this development. The main purpose of the block is to provide a means of making external connections of the indium arsenide chip without the use of flying leads or wire bonds, as discussed in Section II. It also insulates the cooled diode array and the diode copper mounting block from ambient temperatures, as well as providing a smooth vacuum tight surface for mounting the lens barrel. Cooling is accomplished by drawing heat from the array through the copper wafer mount by means of an insulated "cold finger" passing down to the dewar. By proper selection of plastic filler material around the copper mounting bar, the operating temperature of the diode array can be maintained without reducing the external temperature of the plastic block below the surrounding air dew point temperature.

The 50 preamp circuits consist of discrete components soldered to and connected by 25 small printed circuit boards (2" × 1.90") for ease of testing and replacement. Therefore it is necessary to run 50 leads from the array to the outside of the block. This is accomplished by the embedded PC boards that provide fan-out of the detector leads from their 10-mil spacing at the edge of the integrated detector array to 50 mils at the external edge of the block. Two edge-type PC board connectors then mate to these surfaces for connections to the preamp circuitry. If, in future applications, the preamp

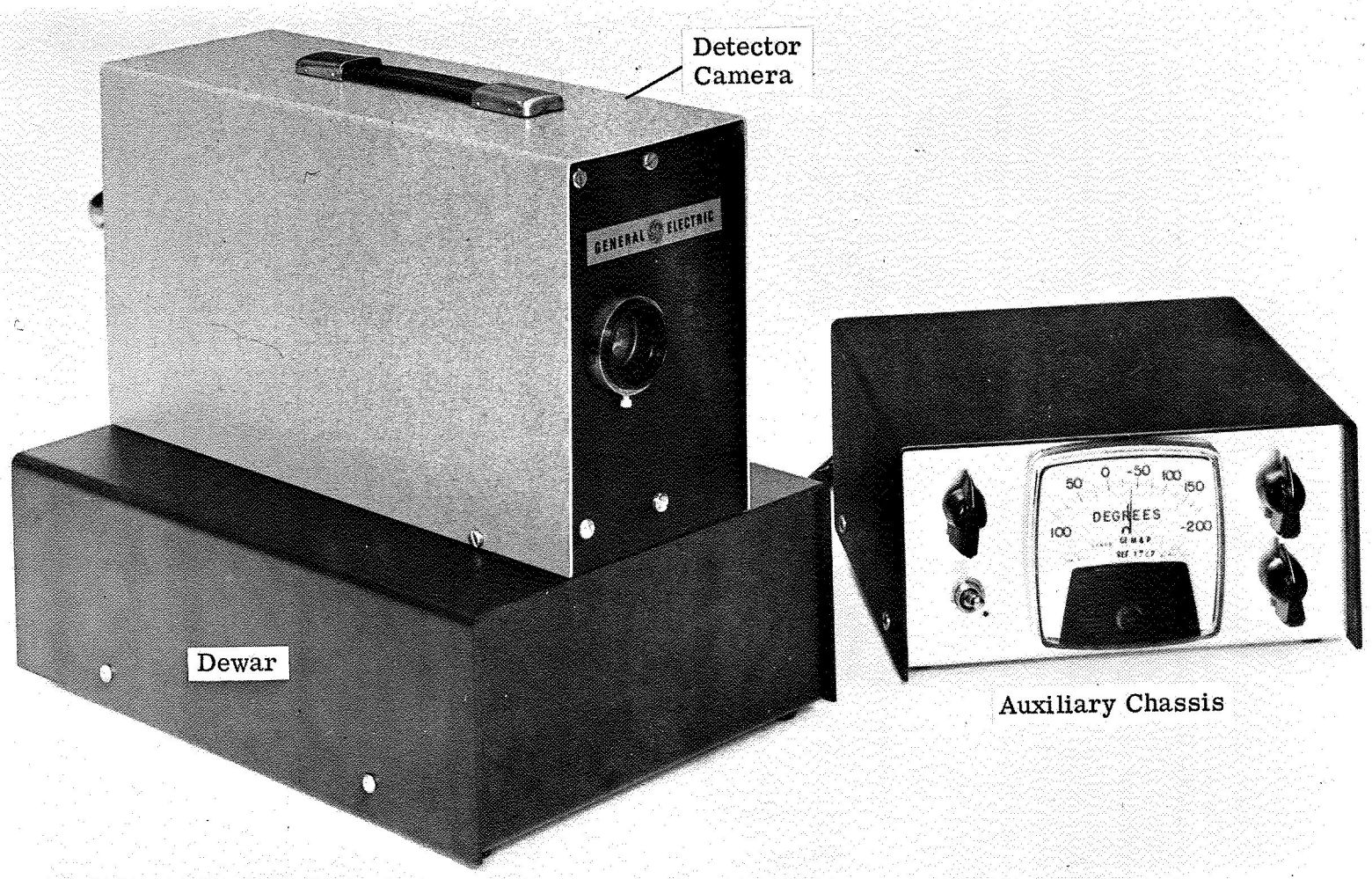

Figure 20. IR Detector System

circuitry can be reduced to integrated circuitry and also embedded in the coplanar surface of the plastic block, the block size can be greatly reduced from that at present. This is possible because the "fan-out" PC boards would be greatly reduced or eliminated since only a few external connections would be required. All other interconnections would be short deposited leads on the coplanar surface, with temperature control of the preamp chips possibly performed by heated copper bars or by insulation. By reducing the size of the plastic block and eliminating the present preamp boards, the entire camera is capable of severe reduction in size and weight. If, in addition, the system is to be designed for space applications and radiation cooling utilized, the dewar may also be eliminated.

Figures 21 and 22 show the detector camera with the cover removed. The 25 preamp circuit boards plug into edge-type connectors mounted to a larger mother board (6.50" × 5.60") that distributes DC power from the 15-pin connector at the rear of the chassis and interconnects preamp circuitry where necessary. Shielded wire connects the preamp connectors to the plastic block connectors, and one RF connector at the rear of the chassis provides the signal output. Three additional standard size PC boards contain scan control circuitry and output interface circuitry for a total of 28 boards in the camera. Color coding permits orientation of the boards in the mother board sockets.

The lens barrel contains a vacuum chamber in front of the array for frost-free operation and also positions an axially adjustable "Iratran 2" lens plus a light chopper attached to the barrel by means of a mounting plate. The components are shown in Figure 23. The vacuum chamber around the diode array is sealed by a silicone "O" ring, and can be pumped down by attaching a 1/4" dia. flexible hose to the brass attachment beyond the check value. The check valve must be open during pumping and closed when the pump is removed. With this vacuum chamber, over (8) hours frost-free operation are possible with a diode temperature of -80°C, assuming the normal temperature and humidity level of laboratory operation. A threaded copper rod or "cold finger" projects through the base of the camera as shown in Figure 24. It is threaded into the tapped hole at the end of the copper wafer mount, and can be removed if it is desired to stand the camera upright without using the dewar. Polyethylene insulation covers both cold finger and wafer mount to prevent condensation within the camera when the cold finger is inserted in the dewar.

2. Dewar and Auxiliary Chassis

The dewar will permit operation of the diodes at temperatures as low as -100°C. Approximately $1\frac{1}{2}$ pints of liquid nitrogen, poured in the 1" diameter top openings, will permit operation for about 2 hours at -80°C, although more liquid nitrogen can be added during operation of the camera. An average insulation thickness of 3/4" polyurethane foam covers the internal aluminum container. There are two additional dewar openings; one in the top for the cold finger and one at the front for vapor boil-off. The vapor boil-off opening can be used for eliminating frost from the IR window, as will be described later.

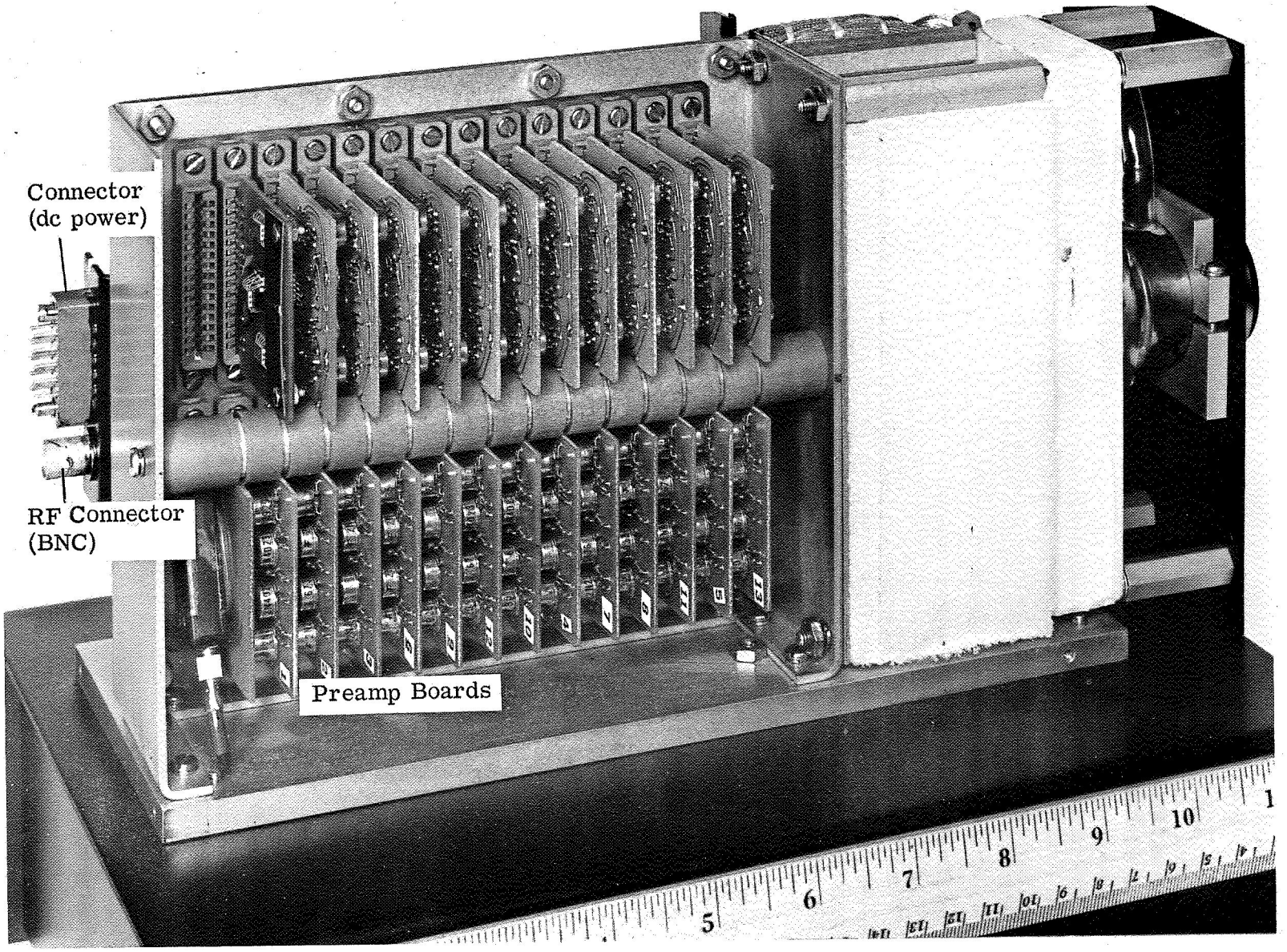

Figure 21. IR Camera with Cover Removed (View 1)

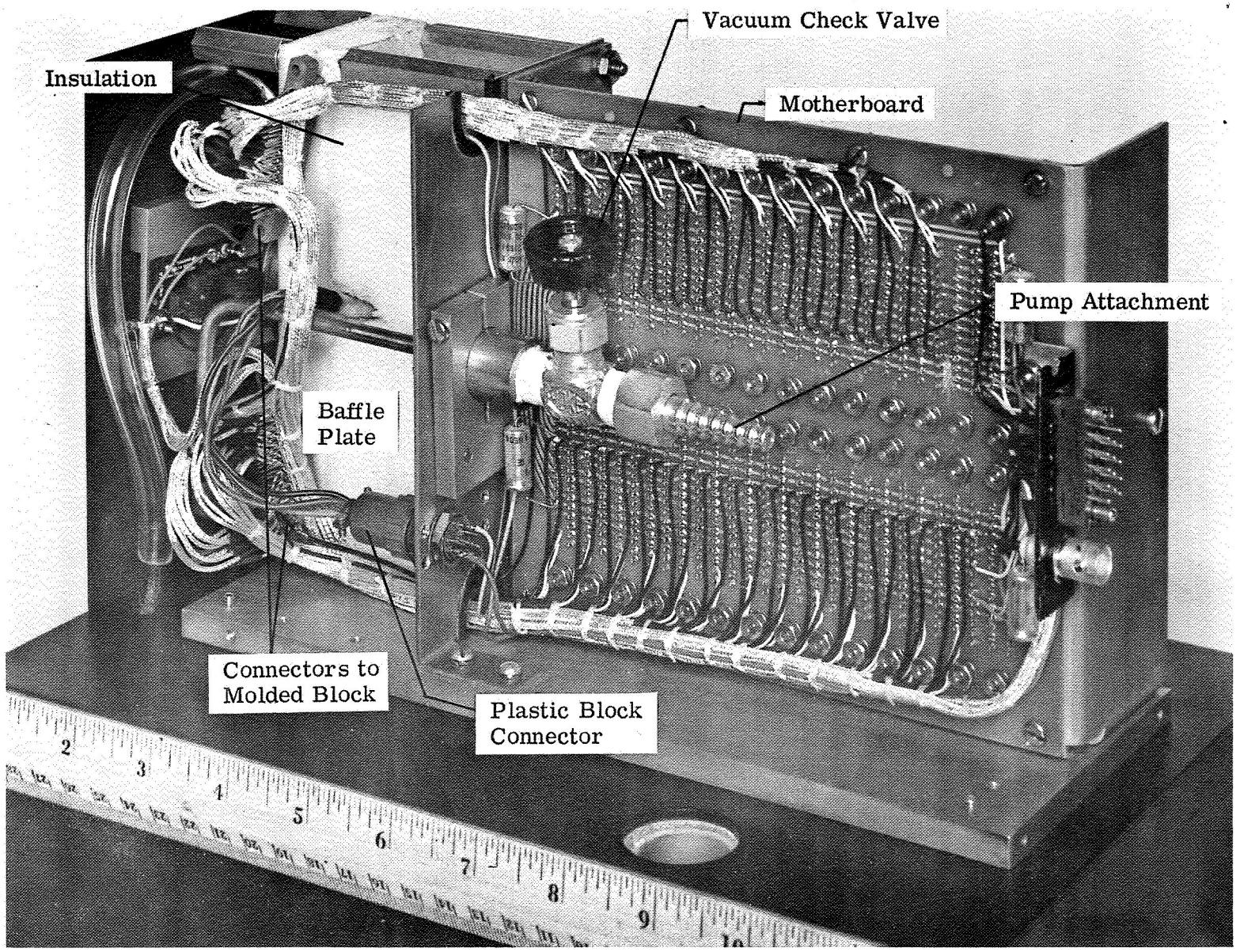

Figure 22. IR Camera with Cover Removed (View 2)

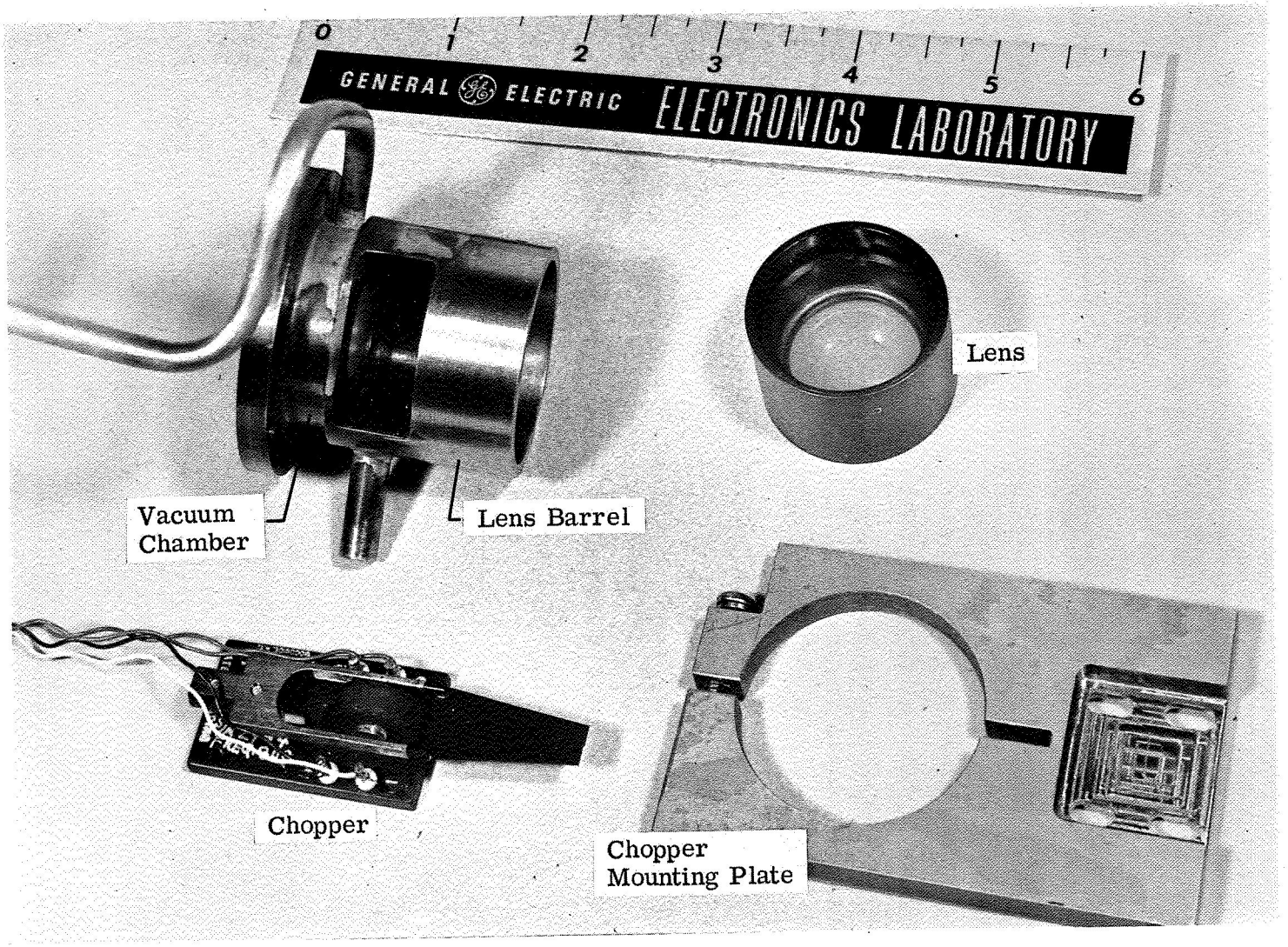

Figure 23. Detector Camera Components

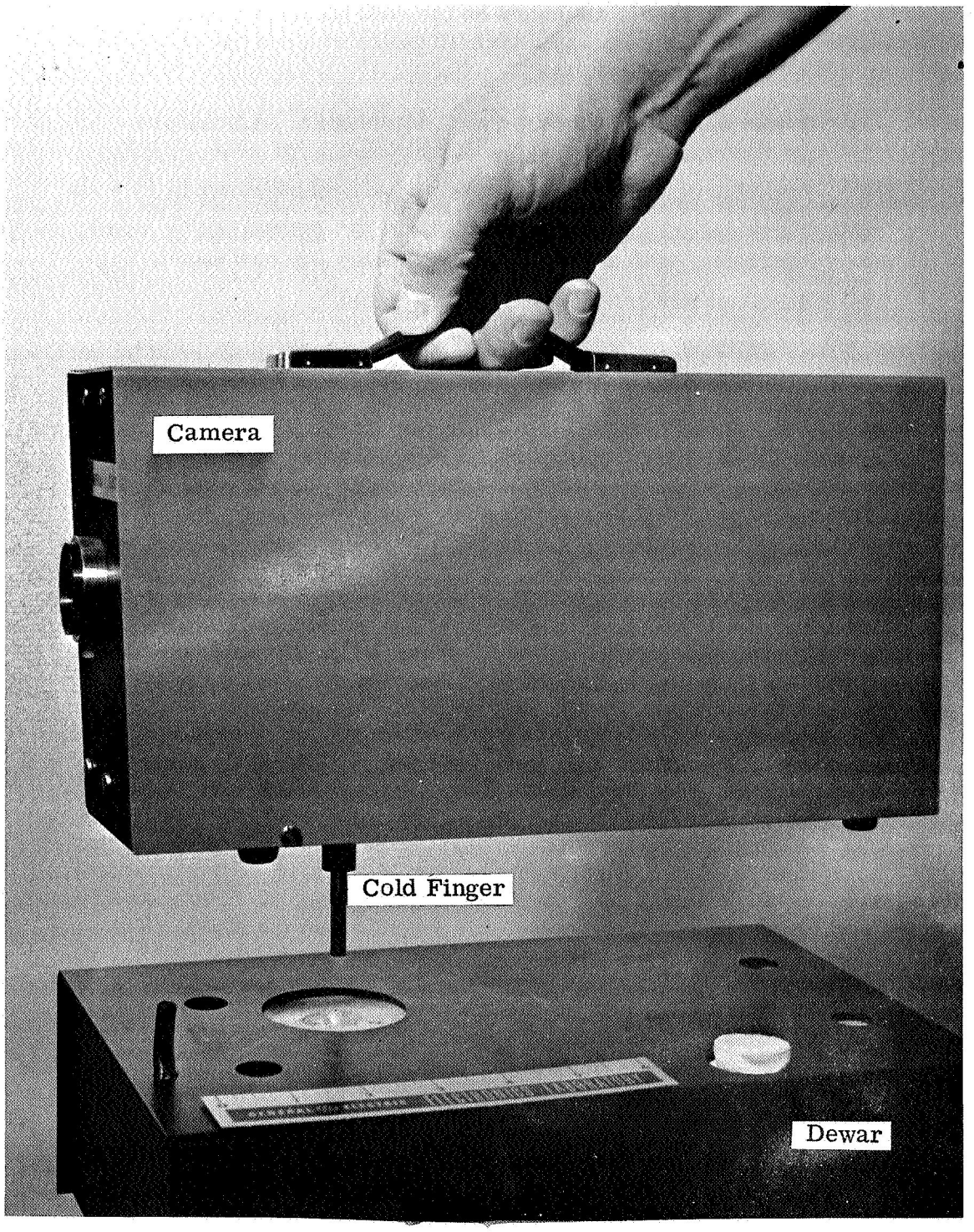

Figure 24. View of Camera Base

The auxiliary chassis provides a convenient carrying case for several functions necessary to the system but not intimately associated with the array circuitry. This unit is connected by a shielded cable to the rear of the camera unit. For operation, a (+5) and (+24) volt power supply source is connected to the marked terminal board on the rear panel. A calibrated temperature meter and an associated potentiometer are mounted on the front panel. In addition, the unit contains:

1) Power supply for the 800-cps light chopper. Adjustment for this supply is through a clearance hole at rear.
2) Two 20-volt, 0.010-amp batteries, adjustable down to 15 volts.
3) Two scan trigger circuits on 2" × 1.90" PC boards, mounted internally, with adjusting potentiometer on front panel.
4) On-off switch for battery on front panel.

Access and removal of all components can be accomplished by removing four screws at the side that hold the cover in place.

B. COOLING

The basic criterion used for design of the cooling system was to obtain operation of the diode array at -80°C for over 1 hour without addition of cryogenic fluid. Liquid nitrogen is used as the cooling fluid because of availability, low cost, and non-corrosiveness. The -80°C temperature is that anticipated for satellite vehicle operation where cryogenic cooling or dewars will not be necessary. The heat loads upon the cooling fluid are almost entirely from conduction or convection through the dewar or cold finger, since the electrical power dissipated at the diodes is negligible.

The diode temperature obtained with the 1/4" dia. cold finger fully immersed in the liquid nitrogen is approximately -100°C. The exact temperature can be read from the thermocouple meter on the auxiliary chassis. The thermocouple leads are iron-constantan and are embedded in the copper diode mount directly behind the diode array. In order to vary the temperature at the diodes to the desired level, two 20-ohm resistors in series are tightly fitted inside the diode mount and connected to the 5v supply. The power input to these resistors can be increased by the potentiometer at the auxiliary chassis, until the final temperature of the array is reached and stabilized as shown on the thermocouple meter.

If higher temperatures than those easily obtained by this method are desired, additional thermal resistance to heat flow from the array to the dewar can be introduced. A fiber washer, for example, can be placed between the cold finger and the diode mounting bar to reduce the number of threads in contact, and thus decrease the heat flow. Conversely, if it is ever desired to obtain a constant temperature below -100°C, a greater heat flow can be obtained in inserting a 1/2" dia. threaded copper bar in place of the present 1/4" dia. bar plus the textolite sleeve.

If the diode array is operated at very cold temperature (below -100°C) or in a very humid atmosphere or both, it is possible that frost may form

on the outside of the IR window sealing the vacuum chamber. This condition can be eliminated by using the gaseous nitrogen boiling from the dewar. A plastic hose is attached to the copper tube at the front of the dewar, and from there to a brazed tube attached to the lens barrel just above the IR window. The small amount of vapor flowing down over the window from this source is moisture-free and will prevent any condensation or frost from occurring on the outside of the window. At the design temperature of -80°C, however, and in a normal air-conditioned atmosphere, this precaution is not necessary. The plastic hose is stored in the front of the dewar chassis, where a coil of copper heats the nitrogen vapor after leaving the insulated liquid chamber.

VI. METEOROLOGICAL APPLICATIONS OF IR DETECTORS

A. WEATHER SATELLITE SIGNAL LEVELS

For the majority of earth surface or cloud temperature measurements from satellites, the 10.5-12 micron band is most useful. A larger percentage of the emittance of objects in the range of 200-300°K lies in this band than in other bands not absorbed by the atmosphere. Emissivity of terrestrial objects generally becomes more uniform and closer to unity at longer wavelengths than 10 microns, which permits a more accurate estimate of surface temperature in the 10.5-12 micron band than at 3.3-4.2 microns. Reflected solar radiation can also be best avoided at longer wavelengths, and daylight as well as night-time measurements can be made from emission only in the 10.5-12 micron band.

However, for objects at higher temperatures such as volcanoes and forest fires, the 3.3-4.2 micron band becomes more attractive because of the larger percentage of emittance and higher detector sensitivity at shorter wavelengths. The numerical advantage can be calculated by comparing the signal-to-noise ratios for each of the spectral bands.

$$\frac{\Delta V_s}{V_n} = \frac{\Delta H}{NEPD}$$

where ΔH is change in irradiance of the aperture (w/cm^2) causing a change in signal voltage ΔV_s and NEPD is the noise-equivalent power density or the value of this irradiance corresponding to the rms noise voltage V_n.

Since $NEPD = NEP/A_o t_o$

$$= \sqrt{A_e \Delta f / D^* A_o t_o}$$

where NEP = detector noise equivalent power (watts)
A_o = collecting optics area = $\pi D^2/4$
t_o = optical transmittance
A_e = detector element area
Δf = electrical bandwidth
and D^* = normalized detectivity

and since

$$\Delta H = \frac{\Delta W t_a A_e}{\pi F^2 D^2} = \frac{\Delta W t_a \theta^2}{\pi}$$

where ΔW is change in object emittance for an object filling the detector field of view θ, t_a is atmospheric transmittance and F is effective f/number.

$$\frac{\Delta V_s}{V_n} = \frac{D\theta t_a t_o D^*(\Delta W)}{4F\sqrt{\Delta f}} \quad .$$

For example, if average D* of an InAsSb detector element is 10^{10} in the 3.3-4.2 micron band, and that for a PbSnTe detector is 10^9 in the 10.5-12 micron band, the relative S/N ratios for short/long wavelength bands is as follows for objects of three temperatures:

T =	301^oK	500^oK	1000^oK
InAsSb / PbSnTe	0.332	8.1	83

Therefore, the InAsSb detector is about 250 times better than the PbSnTe detector for detection of a 1000^oK object than it is for detection of a 301^oK object.

An interesting comparison of 3-4 and 8-12 micron bands for target temperatures near 300^oK was made by Aerospace.[3] This shows that the ultimate superiority of 8-12 micron detectors (supercooled) over 3-4 micron detectors is at least a factor of 4, but that cryogenic requirements and detector production technology strongly favor the 3-4 micron band.

Another comparison can be made of subaperture response or detection of objects smaller than the detector resolution cell. Consider two adjacent surface areas of size A_1. One of these is at background temperature T_o and the other is at the same temperature except for a smaller area A at temperature T. To the system, which is unable to resolve the smaller area, the second surface appears to be at some equivalent temperature T_e. Then if $\Delta T \equiv T_e - T_o$

$$\Delta W_e = 4\sigma T_o^3 p_o \Delta T \quad ,$$

and $$\Delta W_e = \sigma T_o^4 p_o (1-A/A_1) + \sigma T^4 p\, A/A_1 - \sigma T_o^4 p_o$$

solving for pT^4

$$pT^4 = p_o T_o^3 (T + 4TA_1/A)$$

Figure 25 presents the relationship of T and A/A_1 for $\Delta T = 1^oK$, for the two spectral bands of interest. Note that, for 1000^oK, the short wavelength band is about 208 times as effective as the long wavelength band. That is, the ratio A/A_1 is 208 times smaller for 3.3-4.2 microns than the 10.5-12 micron radiation at 1000^oK with 300^oK background.

[3] Hamilton, J.N., "Spectral Regions for Thermal Imaging," Aerospace Corp., January 1966 (AD487978).

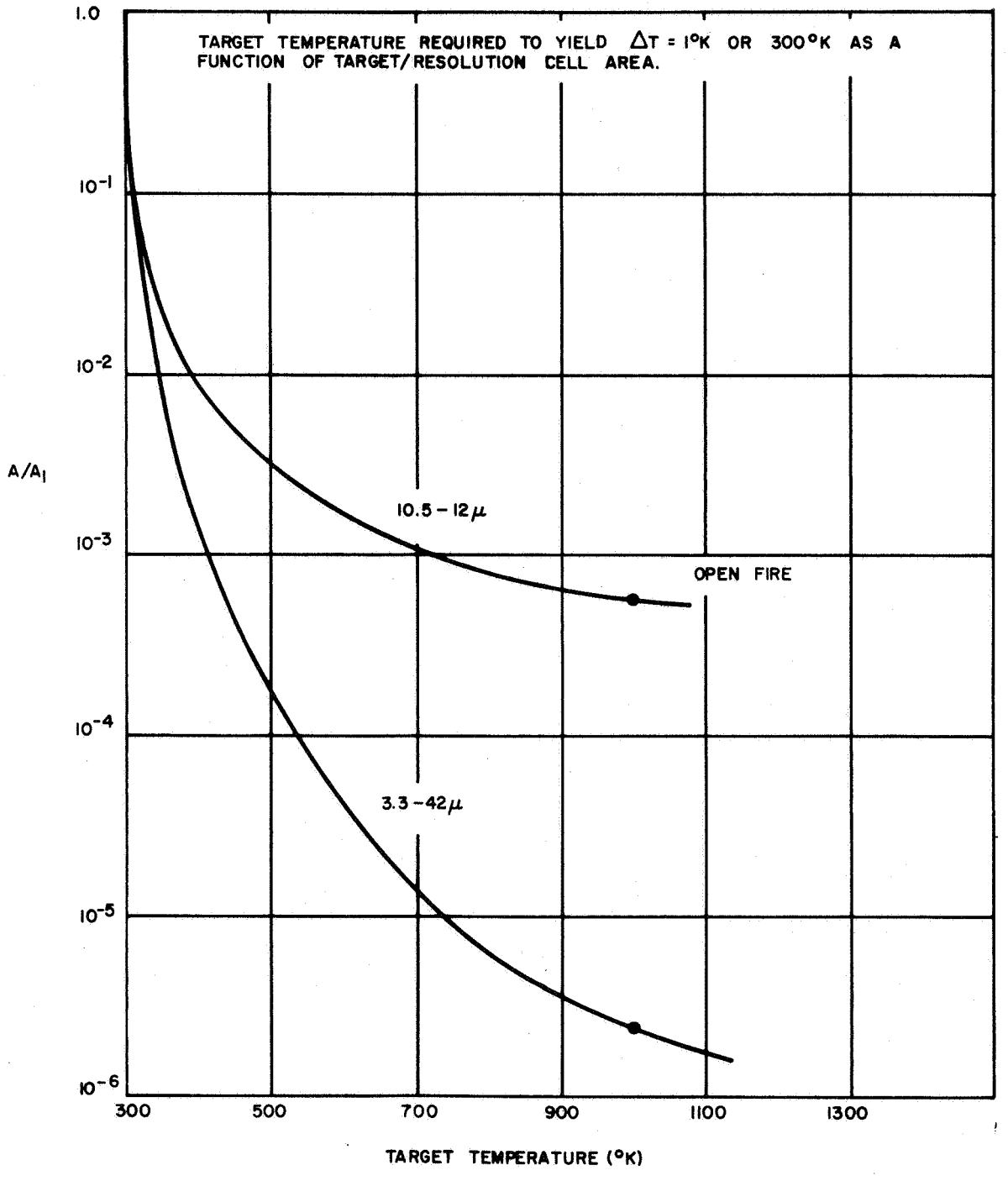

Figure 25. Subaperture Thermal Response

Figure 26 compares the theoretical variation of infared system signal-to-noise as a function of resolved target temperature from 200° to 500°K.

An idealized weather satellite system is assumed with 300°K earth background, optical aperture of 10 inches at f/2, angular resolution of 1 milliradian, optical and atmospheric transmittances of 0.80 and 0.80, and electronic bandwidth of 1 kHz. Two representative spectral bands are selected, 3.3-4.2 and 10.5-12 microns, with typical photodetector sensitivty a factor of ten higher in the short wavelength band.

Note that the short wavelength channel provides higher S/N values only for resolved target temperatures above about 330°K. If the long wavelength sensitivity were a factor of ten higher, or equal to that of the short wavelength channel, the crossover point would move out to about 500°K.

B. COMPARISON OF InAs, InAsSb AND InSb AS 3.3-4.2 MICRON INFRARED SENSORS

The choice of infrared-sensitive material for use in meteorological satellite sensor arrays depends on several factors including target and background spectral emittance, atmospheric and optical transmittance and variations in sensor detectivity with wavelength and operating temperature.

As discussed in the preceeding section, for high target temperatures, the 3.3-4.2 micron band has advantages over longer wavelength bands. In this discussion it was assumed that an InAsSb photodetector would be the best choice in this band. This is probably a reasonable statement, if the properties of this detector can be assumed to be intermediate in spectral response and absolute sensitivity between those of InAs and InSb detectors, as indicated in Figure 27.

If the hypothesized InAsSb detector, which is obviously the best choice, is not obtainable, the choice appears to be between InAs at 200°K and InSb at 77°K. That is, the spectral shift with cooling, of the InAs peak towards shorter wavelengths, produces a lower sensitivity beyond the peak at the lower temperature.

By integrating these spectral response curves together with effective target spectral emittance and atmospheric and optical spectral transmittance curves, the relative signal-to-noise values can be calculated.

The results, listed in Table XII, indicate that InAsSb has a marked advantage over both InAs and InSb, and that InSb has an advantage over InAs, all varying with target temperature and the transparency of the atmosphere. From the extreme cases presented, calculated from 0.1 micron interval data, it can be seen that the improvement factor of both InAsSb and of InSb increases with a decrease in target temperature and with a decrease in the transparency of the atmosphere. These advantages must be compared with the device-operating temperature advantage of InAs, in evaluating the optimum detector material for a particular meteorological application.

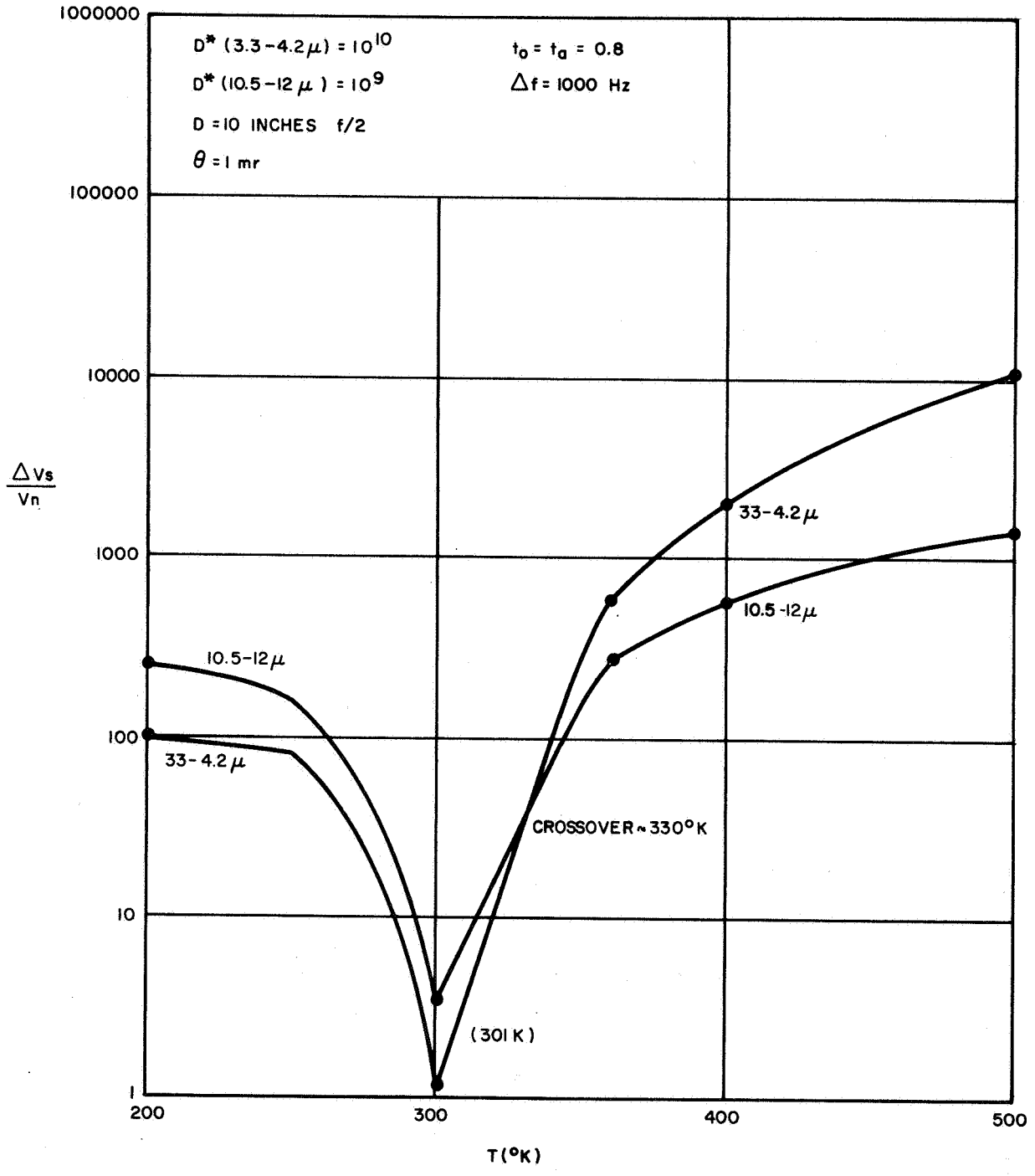

Figure 26. Weather Satellite S/N vs. Target Temperature

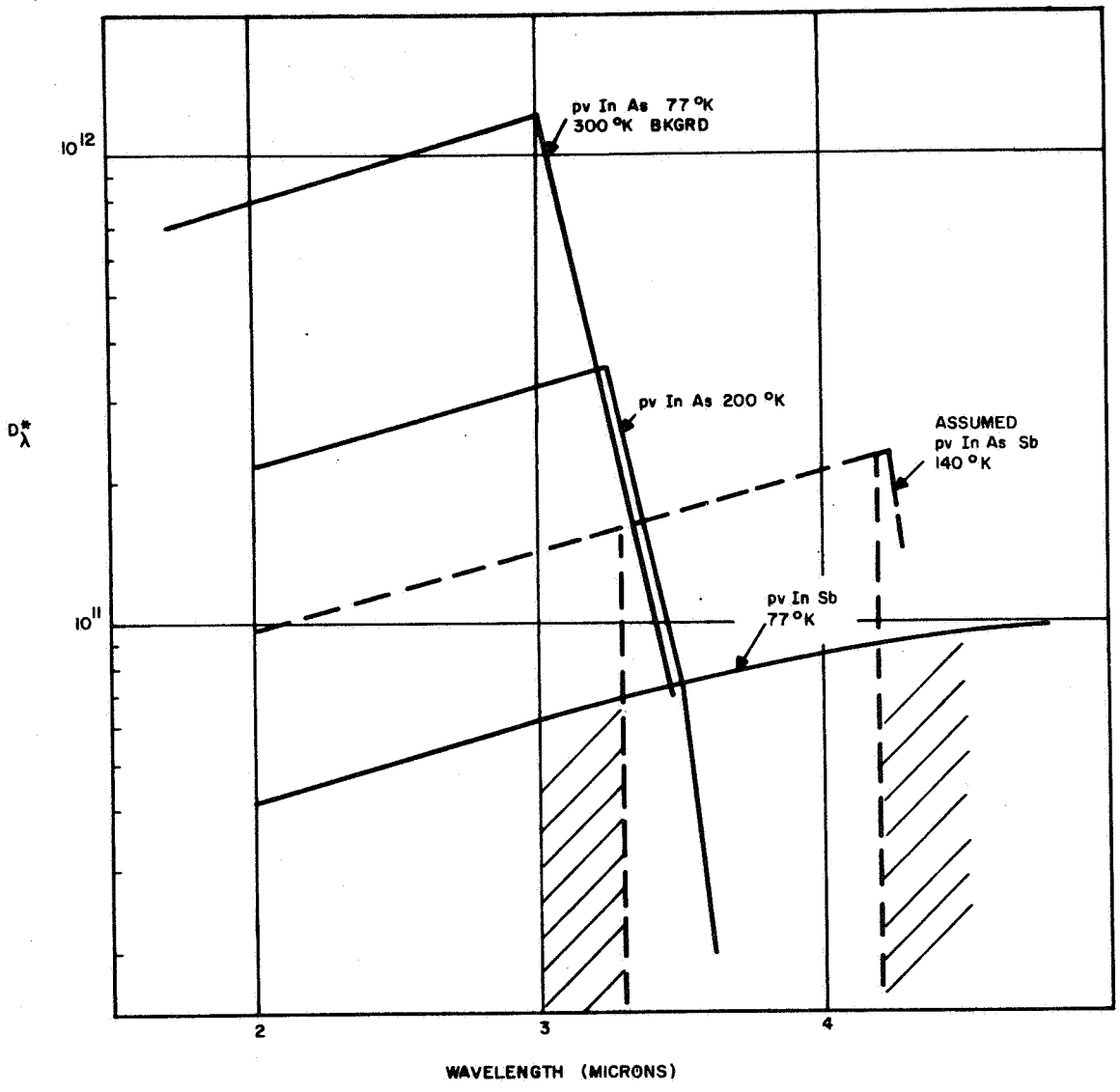

Figure 27. Spectral Detectivity of InAs, InSb, and InAsSb in 3.3 to 4.2 Micron Band

TABLE IX

RELATIVE S/N RATIOS OF POSSIBLE DETECTORS FOR 3.3-4.2 MICRON BAND

A. "GCA" Clear Atmosphere; Visibility, >50 miles; 2 cm H_2O Vapor for One Air Mass

Target Temperature	InAs at 200° K	InAsSb at 140° K	InSb at 77° K
1000° K	1.00	4.26	1.75
350° K	1.00	8.75	3.50

B. "Altshuler" Computed Standard Atmosphere M.R. = 7 km; T_o = 300° K; 4.1 cm H_2O

1000° K	1.00	6.70	2.70
350° K	1.00	13.70	5.49

VII. NEW TECHNOLOGY APPENDIX